GAIN CONTROL AND LINEARITY IMPROVEMENT FOR

LOW NOISE AMPLIFIERS IN 5GHZ DIRECT CONVERSION RECEIVERS

By

MALLESH RAJASHEKHARAIAH

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To the Faculty of Washington State University:

The members of the Committee appointed to examine the thesis of MALLESH RAJASHEKHARAIAH find it satisfactory and recommend that it be accepted.

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Chair

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GAIN CONTROL AND LINEARITY IMPROVEMENT

FOR LOW NOISE AMPLIFIERS IN 5GHz DIRECT CONVERSION RECEIVERS

Abstract

by Mallesh Rajashekharaiah
Washington State University
May 2005

Chair: Deukhyoun Heo

The unprecedented growth in wireless technology has served to create an ever-increasing need for lower power, higher performance, and low cost receiver topologies. Apart from performance enhancement, recent times have also seen an increase in newer topologies catering to multi-mode receivers featuring reconfigurability. From multi-band to multi-gain, the spectrum is broad. Also with the advent and success of complementary metal oxide semiconductor (CMOS) technology, primarily owing to its economic feasibility, topological innovation is a hard requirement in order to match the performance standards set by high-performance technologies like GaAs and SiGe. CMOS technology has also made possible the creation of feasible System-On-a-Chip (SOC) solutions for higher integration needs. The need for multi-mode receivers is felt even more strongly with SOC solutions becoming more feasible.

This dissertation explores the design of a multi-mode receiver front end component, viz. the Low Noise Amplifier (LNA). A LNA having a noise figure of 3.1dB, with dual-mode operation and a new integrated gain controllable on-chip active balun, have been designed in 0.25-um CMOS technology for a 5 GHz Industrial Scientific Medical (ISM) band direct conversion receiver (DCR). The circuit consumes 10mA of current in the high gain mode giving 20dB of gain while using 50% less power in the low gain mode and providing a gain of 12 dB. With the active balun having gain and phase mismatch within 0.5dB and 1 degree, respectively, the presented circuit is believed to be the first to integrate an LNA, gain controllability and an

on-chip active balun, paving the way for higher silicon real estate efficiency in future designs. Measurement details for the LNA and active balun are presented and discussed.

The thesis also explores the needs and theory behind receiver and LNA linearity. Different linearity enhancement techniques are discussed followed by the introduction of a novel enhanced third order transconductance (g_{m3}) cancellation technique. An enhanced linearity LNA, designed using this technique is presented and analyzed. Advantages of this architecture are discussed and simulation results are shown along with the submitted layout.

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2. Rajashekharaiah, M., Upadhyaya, P., Deukhyoun Heo, E.Y.Chen, “A 5GHz LNA with New Compact Gain Controllable Active Balun for ISM band applications” *International Conference on Solid-State and Integrated Circuits Technology 2004,* Beijing , 18-21 Oct, 2004.

3. Rajashekharaiah, M., Upadhyaya, P., Deukhyoun Heo, E.Y.Chen, “A compact 5.6 GHz low noise amplifier with new on-chip gain controllable active balun” *IEEE Workshop on Microelectronics and Electron Devices*, pp.131-132, April 2004

4. Upadhyaya, P., Rajashekharaiah, M., Deukhyoun Heo, E.Y.Chen, “A New 0.25-um CMOS Doubly Balanced Sub-Harmonic Mixer for 5-GHz ISM Band Applications” *International Conference on Solid-State and Integrated Circuits Technology 2004,* Beijing , 18-21 Oct, 2004.

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7. Mallesh Rajashekharaiah, Parag Upadhyaya, Deukhyoun Heo, Emery Chen, "A New Gain Controllable On-Chip Active BALUN For Direct Conversion Receiver", *International Symposium on Circuits And Systems* - ISCAS 2005 at Kobe, Japan in May 2005.

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Dedication

To my family

ABBREVIATIONS

AC Alternating current

ADC Analog-to-digital converter

AGC Automatic gain control

AM Amplitude modulation

BER Bit-error rate

BiCMOS Bipolar complementary metal oxide semiconductor

BJT Bipolar junction transistor

BPF Bandpass filter

CMOS Complementary metal oxide semiconductor

CLK Clock

DC Direct current

DCR Direct-conversion receiver

DGLNA Dual gain low noise amplifier

DSP Digital signal processor

ESD Electrostatic discharge

F Noise factor

FER Frame error rate

GCAB Gain controllable active balun

HGM High gain mode

HPF Highpass filter

IC Integrated circuit

IF Intermediate frequency

IIP2 Second-order input intercept point

IIP3 Third-order input intercept point

I/Q Inphase/Quadrature

ISM Industrial, scientific and medical

LC Inductor-capacitor

LGM Low gain mode

LNA Low-noise amplifier

LO Local oscillator

MOS Metal oxide semiconductor

NF Noise figure

NMOS N-channel metal oxide semiconductor

OIP3 Third-order output intercept point

PCB Printed circuit board

PMOS P-channel metal oxide semiconductor

RC Resistor-capacitor

RF Radio frequency

RX Receiver

SFDR Spurious free dynamic range

SiGe Silicon-germanium

SNR Signal-to-noise ratio

TX Transmitter

VCO Voltage controlled oscillator

WLAN Wireless local area network

2G Second generation

3G Third generation

CHAPTER ONE

INTRODUCTION

1.1 Background and Motivation

Ever since Guglielmo Marconi succeeded in sending wireless signals over a small distance in his laboratory in 1895, wireless communication has never looked back. The growth and development of human knowledge in the area of wireless communication has grown in leaps and bounds since then and with the tremendous growth in the wireless industry in the recent years, there has not been a better time for the air to make waves. While early work targeted successful, error-free transmission of data, the trend has changed towards achieving higher integration and lower costs, with the advent of the integrated circuit technology era, while continuing to improve on all the performance parameters of wireless systems. The age of the semiconductor has seen a further boost in this direction, with decreasing feature lengths and deep sub-micron technology. The demand for higher integration level keeps growing in order to keep operating costs low and to realize compact and low cost wireless products which are also power efficient.

Any wireless system essentially consists of a transmitter, a receiver and a medium. This dissertation will primarily focus on the receiver part of a wireless system with emphasis on an important front-end component, the low noise amplifier (LNA). Wireless or radio frequency (RF) receiver architectures can be primarily divided into heterodyne and homodyne architectures. In heterodyne architecture, the received signal band is translated to a much lower frequency so as to relax the Q required for the channel select filter. On the other hand, in a homodyne or direct conversion receiver (DCR), the signal is translated to a near-zero or DC frequency using a mixer circuit. Although the principal of operation is similar in both the architectures, the challenges and requirements of both vary considerably. While heterodyne receivers suffer from image rejection and integration problems, the homodyne receivers have DC offset issues which directly impact the performance of the mixer. However, the simpler homodyne architecture offers the important advantages of circumventing image problems and

second, subsequent down-conversion stages in the receiver can be low pass filters and baseband amplifiers that are more amenable to monolithic integration. As far as the operation and functionality of the low noise amplifier is concerned, the major differences will be in terms of the output load and matching, I/Q mismatch, in case of an integrated active BALUN and spurious interference levels. The primary purpose of an LNA is to improve the signal-to-noise ratio (SNR) of the receiver by providing amplification or gain to the low-amplitude received signal, while not contributing significantly to the existing noise. Apart from gain, there are several performance parameters of importance that need to be addressed and the details will be discussed in chapter 2.

Further more, the market share for gain controllable RF transceivers featuring power-efficient RF components has seen significant growth. State of the art in wireless transceivers features an LNA with gain control capability. The gain controllability feature is required to properly handle different signal strength levels at the receiver's input. Strong and dynamic (time varying) signal strength at the front end of the receiver due to fading effects and reflection from moving objects, (See Fig.1), can saturate the receiver or can degrade the receiver's signal to noise ratio. The gain controllability in the receiver front-end can mitigate this problem.

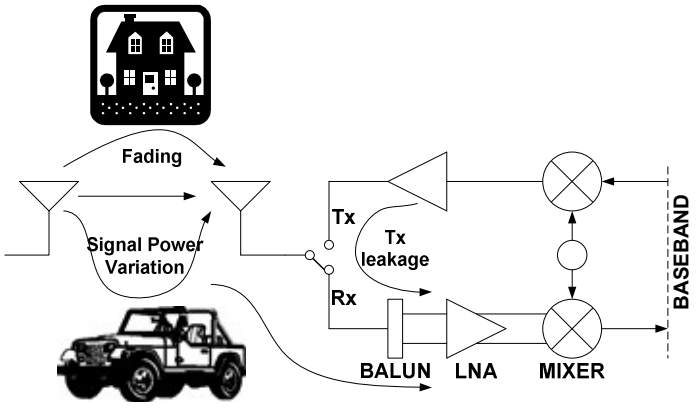


Figure 1. Fading and interference mechanisms

Balanced and symmetrical design presents a circuit designer with the advantages of keeping the common mode substrate noise at a minimum due to the inherent properties of a differential circuit. Similarly, in RF circuit design, a balanced architecture is preferred to an

unbalanced one owing to its higher insensitivity to substrate and other noise sources. However, since an incoming RF signal is an unbalanced one, it is often desirable to split this into two differential signals opposite in phase and equal in amplitude and this is typically done using a BALanced to UNbalanced signal converter or BALUN. Conventionally, passive components have been used to implement the balun. However, owing to the size of passive baluns, they are unsuitable for integrated circuit applications. Apart from being bulky, passive components are relatively lossy compared to their active counterparts and loss of signal power is highly undesirable in RF circuits especially at the input stages where signal amplitude is very low. Typically the use of passive components limits the bandwidth of baluns for RF circuits, which usually need broadband operation. Further more, when a BALUN is used as the first component of the receiver, its high noise level can be detrimental to the receiver SNR. The same applies when it's used between the LNA and mixer, but to a lesser extent. This promotes the need for active BALUN circuits that are not lossy, do not contribute significantly to the noise and are non-bulky.

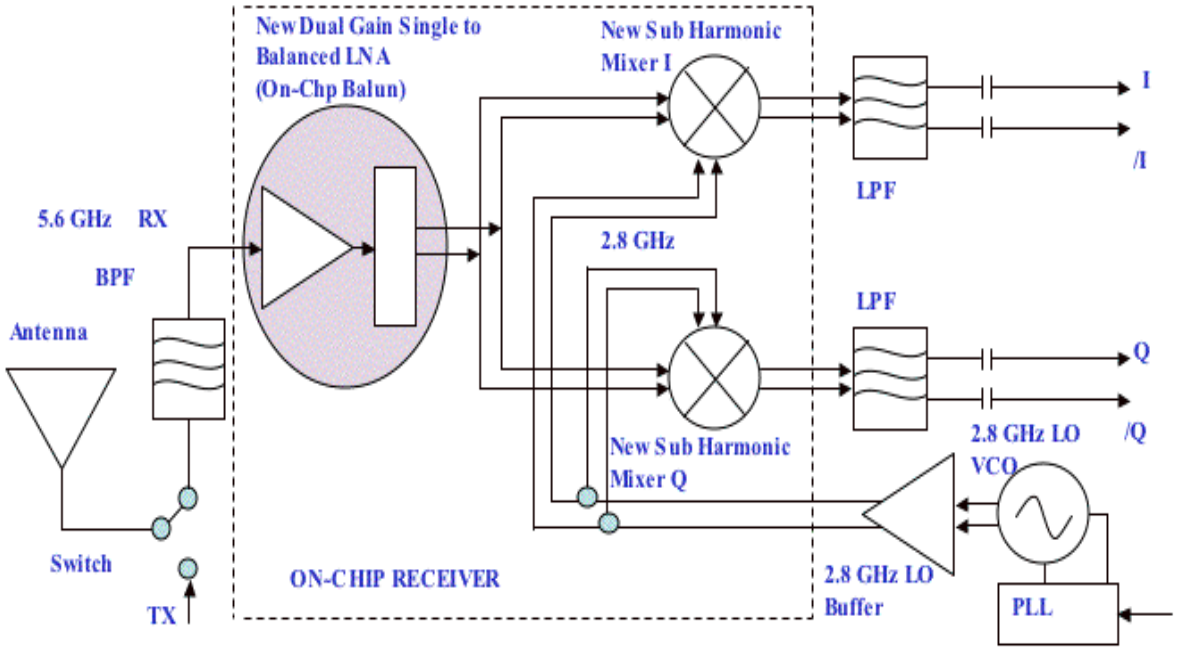


Figure 2. Proposed LNA with Active Balun for proposed DCR

The proposed architecture in this work is a step in this direction and introduces a compact structure which eliminates a passive balun that is required in a receiver (See Fig.2) and goes a step further by adding gain a controllability feature to it, in order to mitigate saturation problems as explained earlier. The dual gain LNA (DGLNA) integrates a dual gain controllability feature and an active balun into a LNA, where the low gain mode (LGM) provides 50% power savings compared to the high gain mode (HGM).

Having established the motivation and background for the research work undertaken by the author, the following chapters will go into details about the LNA design and performance.

1.2 Thesis organization

The dissertation will be presented in six different chapters. The first chapter introduces the topic of research and includes a brief about the publications from the author's research efforts. Chapter two builds on the introduction by delving into details about performance parameters of an LNA, the design challenges and trade-offs involved. Chapter three completes the literature review by looking at current research in this area, highlighting the state of the art in LNA design. Chapters four and five explain in detail the work accomplished by the author highlighting technical achievements with theoretical background. Finally chapter six will showcase the results of this work, followed by the conclusion and bibliography.

CHAPTER TWO

LNA – PERFORMANCE PARAMETERS AND DESIGN CHALLENGES

2.1 Performance parameters for a low noise amplifier

The design of an LNA, being a vital component of the RF receiver front-end, is guided by several design principals aiming to achieve maximum performance for each important parameter. This chapter lists and explains the various performance parameters for an LNA and the impact they have on the overall receiver performance. The focus on the parameters will be considering the application of the LNA to a DCR. A general block diagram of a DCR is shown in Fig.3 with the assumption of same transmit and receive bands.

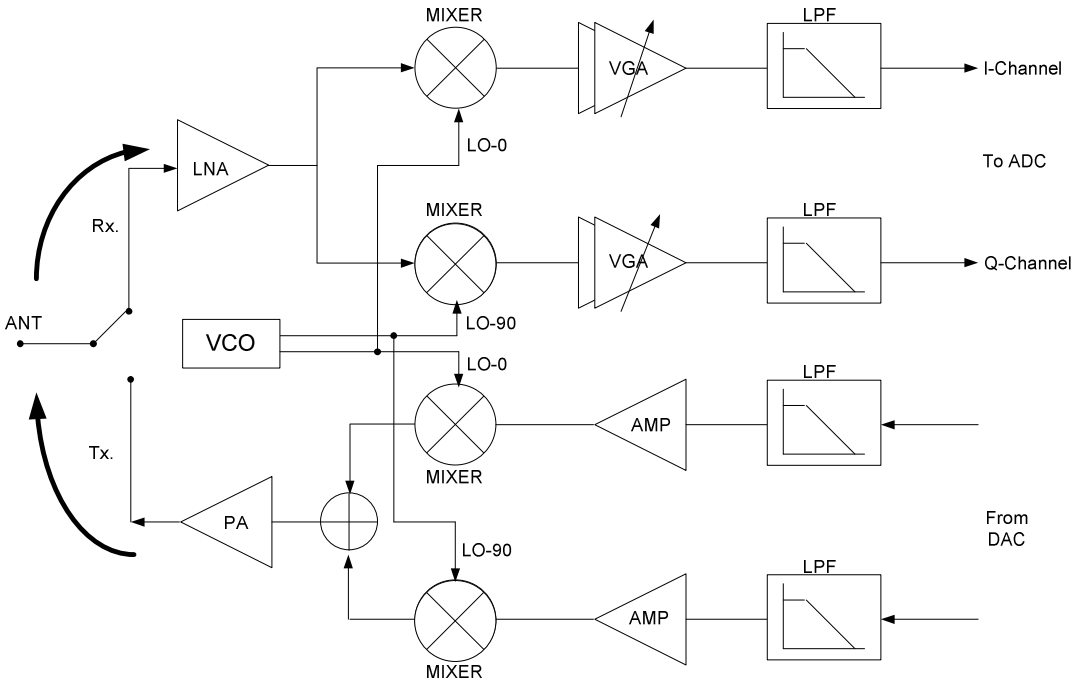


Figure 3. General block diagram of a direct conversion receiver

The LNA's figure of merit for performance evaluation includes noise figure, gain, linearity (P1dB, IIP3), power consumption, and silicon real estate in order of importance.

2.1.1 Small signal gain

As an amplifier, the gain provided by the LNA is one of the most important parameters. Owing to the fact that an incoming RF signal is of relatively small amplitude, the small signal gain of the LNA is a more important gain indicator than the large signal gain. Small signal gain of the LNA is indicated by the S-parameter S21. Multiple stages of the LNA may be employed often in order to increase the gain level of this primary receiver stage. A high gain in the first stage of the receiver offsets the noise contributions of the stage to a certain extent. However, the noise figure is a far better indicator of the noise performance of the LNA and will be explained in the following section.

2.1.2 Noise figure

Another vital performance parameter for a 'low noise' amplifier is the noise figure. It indicates the noise contribution of the LNA stage to the overall receiver noise. The noise figure impacts the signal sensitivity of the amplifier. Sensitivity is the minimum signal strength that can be sensed and processed by the amplifier with a minimum signal quality usually determined by bit error rate or frame error rate (BER/FER), and is given as,

$$Sensitivity = kT(dBm) + 10\log B + NF(dB) + SNR_{\min} \tag{2.1}$$

The product kT at 290 K is -174dBm and is the noise power level at a particular temperature, B is the bandwidth, NF is the noise figure and SNR_{min} is the minimum signal to noise ratio required to process an incoming signal. From the above equation, the NF can also be deduced accordingly. Thus the lower limit on signal detection is set by the noise floor and the noise figure of the component, while the upper limit is determined by the 1-dB gain compression point, which will be explained in the following sections.

The noise contributed by the LNA is the most dominating factor in the overall noise figure of the receiver. This can be understood by looking at the Frii's equation given in (2.2).

$$F = F_1 + \frac{F_2 - 1}{G_1} + \ldots + \frac{F_N - 1}{\prod_{i=1}^{N-1} G_i}, \tag{2.2}$$

where F is the receiver noise figure, Fi is the noise figure of i^{th} stage and Gi is the gain of i^{th} stage. When conceived for a typical receiver chain including the LNA as the first element followed by mixer and so on, (2.2) can be written as (2.3), as shown below.

$$Freceiver = F_{LNA} + \left({F_{Mixer} - 1} \Big/ {Gain_{LNA}} \right) + \cdots + \left({F_{n-1}} \Big/ {Gain_{LNA} * Gain_{Mixer} * \cdots Gain_{n-1}} \right) \tag{2.3}$$

As seen from (2.3), the LNA noise dominates the overall noise figure as the contribution of all other stages is decimated by the gain of the preceding stage. Thus, to reduce the total noise, firstly, the LNA itself should have low NF and secondly, it should provide high gain to reduce noise impact of the mixer.

Further, the NF of an LNA can be expressed as a function of the four basic noise parameters, usually provided by a manufacturer. The four parameters are listed in table below followed by their relationship to NF.

TABLE I

NOISE PARAMETERS

NF_{min}	Minimum Noise Figure
r_n	Noise Resistance
G_{opt}	Real part of optimum source admittance ($Y_{opt} = G_{opt} + jB_{opt}$)
B_{opt}	Imaginary part of optimum source admittance

$$NF(y_s) = NF_{\min} + \left(\frac{r_n}{G_s} \right) * \left| y_s - y_{opt} \right|^2 \tag{2.4}$$

The minimum noise figure is a function of the technology in consideration, while r_n is the spectral density of a noise generator represented quantitatively in units of resistance. G_{opt} and B_{opt} are the real and imaginary parts of the optimum source admittance.

Noise in LNAs is a result of different contributing factors like thermal noise, shot noise and flicker noise. The most dominating of these factors is the thermal noise. When there is no bias, there is supposed to be a thermal equilibrium in the active device. Once a bias is applied, carrier collisions cause diffusion noise and are in agreement with Johnson's thermal noise model, hence the name thermal noise. Based on the fact that the MOSFET is a modulated resistor, capacitively coupled to the gate, thermal noise model for MOSFETs was proposed by Van der Ziel, which consists of drain current noise (i_d), induced gate current noise (i_g), and their cross-correlation coefficient as shown below [1]:

$$\overline{i_d^2} \triangleq 4kT\,\Delta f\,\gamma g_{d0} \tag{2.5}$$

$$\overline{i_g^2} \triangleq 4kT\,\Delta f\,\delta g_g \tag{2.6}$$

$$\overline{i_g i_d^*} \triangleq c\sqrt{\overline{i_g^2 i_d^2}} \tag{2.7}$$

$$g_g \triangleq \xi \frac{\omega^2 C_{gs}^2}{g_{d0}} \tag{2.8}$$

where γ, δ, and ξ are bias-dependent factors; g_{d0} is the drain output conductance under zero drain bias; g_g is the real part of the gate-to-source admittance; and c is the cross correlation coefficient. The induced gate current noise is thermal noise that is induced by local fluctuations in the channel via capacitive coupling through the gate oxide. Induced gate noise is proportional to f^2, owing to the ωC dependence, while drain noise is frequency independent i.e. white noise. The induced gate noise dominates noise performance of MOSFETs at high frequencies. For long channel MOSFETs, γ satisfies the inequality, $2/3 < \gamma < 1$. The value of 2/3 holds when the MOSFET is in the channel pinch-off region, and the value of 1 is valid when the drain bias is zero [2]. Also for long channel MOSFETs in saturation, δ, c and ξ are reportedly 4/3, *j*0.395, and

0.2 [3], respectively. This model agrees well with long channel MOSFETs down to 1.7μm. Substantial increases have been observed in γ and δ for MOSFETs with shorter channel length.

Other noise sources like shot noise and flicker noise hold more importance in circuits like voltage controlled oscillators and mixers. Shot noise is dominant only in the sub-threshold region of the device operation because of the carrier transfer involved, as in junction devices. Flicker noise, also known as *1/f* noise has a spectral density that is inversely proportional to the operating frequency, and caused primarily because of charge trapping by defects and impurities. As far as the noise figure of LNA is concerned, a designer should be concerned with the thermal noise models provided with the device models.

2.1.3 1-dB gain compression point

The input power value, in dB, at which the gain of the LNA drops by 1 dB, is referred to as the 1 dB gain compression point or the P1dB. This parameter is important for an amplifier circuit as it gives an idea about the maximum input power that the circuit can handle by providing a fixed amount of gain. Once the input power exceeds the P1dB of the amplifier, the gain starts decreasing. This can be understood by considering the amplifier as a nonlinear memory-less time-invariant system, where the output *y(t)* is expressed in terms of the input *x(t)* as,

$$y(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + \cdots \tag{2.9}$$

If $A\cos(\omega t)$ is applied as the input to such a system, ignoring the higher order terms, the output will be,

$$y(t) = \frac{\alpha_2 A^2}{2} + \left(\alpha_1 A + \frac{3\alpha_3 A^3}{4} \right) \cos(\omega t) + \frac{\alpha_2 A^2}{2} \cos(2\omega t) + \frac{\alpha_3 A^3}{4} \cos(3\omega t) \tag{2.10}$$

As seen from (2.10), the fundamental frequency component is also dependent on the third order term, A^3. Hence when α_3 is opposite that of α_1, the output starts to decrease. This effect is also of

importance when we discuss the third order intermodulation terms in the following section. Thus, it's desirable that an LNA should have as high a P1dB value as feasible without significant tradeoffs in the other parameters. For receivers the P1dB is calculated with respect to the input while for transmitters it's referred to the output, for obvious reasons.

2.1.4 Linearity and IIP3

Linearity is an important parameter for a receiver front end component, such as the LNA. Linearity of an LNA is a measure of the intermodulation distortion that it experiences due to the presence of unwanted spurious signals in the vicinity of the desired frequency band. Consider two nearby signals, ω1 and ω2 in a nonlinear system, that produce third order components, $2\omega_1$- ω_2 and $2\omega_2$- ω_1 on combination. If the difference between the two signals is small, then the resultant third order signal components will appear in vicinity of the fundamental signals. Now, if a desired weak signal is accompanied by two strong interferers, the resultant third order component may appear in the desired signal band, as shown in Fig 4. This third order intermodulation corrupts the desired signal thereby causing bit and frame errors which is a highly undesirable phenomenon in RF circuits.

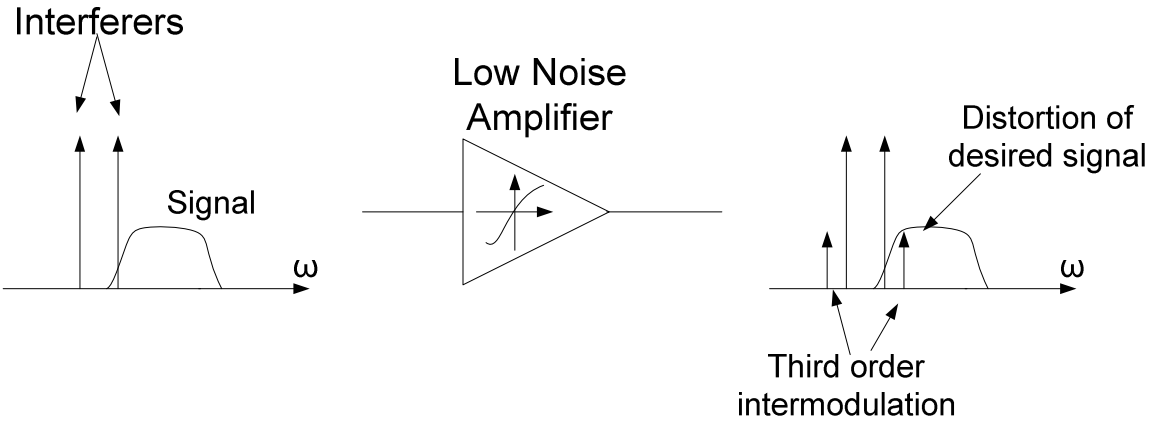


Figure 4. Intermodulation distortion due to strong interferers near desired signal

A popular measuring parameter for intermodulation distortion levels is the third order intercept point or IP3. The IP3 can be measured using a simple two-tone test in which the value of A is chosen to be sufficiently small so that higher order nonlinear terms are negligible and gain is relatively constant and equal to α_1. As A increases, the fundamentals increase in proportion to A, while the third order components increase in proportion to A^3. When plotted on a logarithmic scale, the slope of third order IM products is three times that of fundamental (See Fig 5). The point at which the extrapolated curves meet is called the third order intercept point or IP3. The vertical coordinate of this point is called the output IP3 or OIP3 and the horizontal coordinate is called the input IP3 or IIP3.

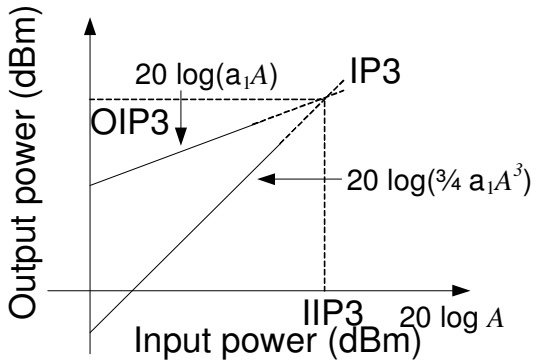


Figure 5. Third order intermodulation measurement

The IIP3 is a very effective measure of the circuit linearity, more than simple IM measurement. If the magnitude of IM products is used as a measure of linearity, then the input amplitude needs to be specified. On the other hand, the IIP3 by itself can be a unique means of comparing linearity of different circuits. The higher the IIP3, the more linear the circuit. This dissertation will also discuss linearity enhancement techniques for CMOS LNAs and propose a novel technique to do so in Chapter 5.

2.1.5 Input and output matching

Input and output impedance matching are also important aspects of LNA design useful in containing signal loss at the input and the output ports by means of reflection. The need for matching arises because amplifiers, in order to deliver maximum power to the load, or to perform in a certain desired way, must be properly terminated at both the input and the output ports. In RF circuits, characteristic impedance matching is necessary in order to assure minimum signal loss at the ports. The characteristic impedance in this case is 50 Ω for maximum transfer of power from port to port.

Typical matching networks are 'T' or '∏' LC networks with values arrived upon by using the smith chart for impedance matching. Detailed explanation on the topic can be found in any introductory book on RF circuits. Matching networks can be implemented on-chip or off-chip depending on the need for characterization, performance concerns and flexibility. Section 2.2.2 explains a few typical input matching networks and the trade-offs involved with each. It then continues to explain the theory behind the source degeneration matching used in the DGLNA. Inter-stage matching is another crucial aspect of a multi-stage amplifier design. In spite of good input and output matching, if the inter-stage matching is not reasonable, the signal loss will make the circuit performance low. Typically, inter-stage matching is done on chip because of the inaccuracies involved with off-chip matching.

2.1.6 Stability

In addition to all the major performance parameters, the stability of the LNA is a basic requirement if the circuit is to operate as expected without undesirable oscillations which could practically destroy the active devices due to voltage buildup. The stability factor, *K*, is a popular measure of circuit stability. A value greater than 1 for K and less than 1 for $|\Delta|$ is the necessary

and sufficient condition for unconditional stability meaning, the circuit will be stable under any load condition. The value of K is obtained from,

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{2.11}$$

While Δ is given by,

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| \tag{2.12}$$

Thus the set of conditions, K>1 and |Δ|<1, indicate unconditional stability for a two-port network. Stability circles are useful tools in circuit design to evaluate the stabile region for a particular load on the two-port network.

2.2 Design challenges

In this section various design challenges and design trade-offs associated with the design of a low noise amplifier are considered. We shall also cover some popular LNA topologies, their pros and cons and additional topics of interest like loading and biasing.

2.2.1 Gain and noise matching tradeoffs

One of the typical tradeoffs involved in LNA design is that of the balancing between good gain matching, while maintaining low NF. The basic reason that such a tradeoff exists, lies in the fact that F_{min} and Γ_{opt} points are at different locations. Here F_{min} is the minimum noise figure and Γ_{opt} is the optimum reflection coefficient. The source admittance at which minimum noise figure, F_{min}, is achieved is called the optimum source admittance, y_{opt}, and is related to the optimum reflection coefficient as,

$$y_{opt} = \frac{1 - \Gamma_{opt}}{1 + \Gamma_{opt}} \tag{2.13}$$

The optimum source reflection coefficient point, Γ_{opt}, indicates a point of maximum gain, while the optimum source admittance, y_{opt}, indicates a point of minimum noise figure, F_{min}. But the catch is that, these two points are not nearby and call for an intermediate point in between, thereby leading to a tradeoff. y_{opt} as mentioned in section 2.1.2 is given by,

$$y_{opt} = G_{opt} + jB_{opt} \tag{2.14}$$

2.2.2 Stable input matching and low NF

In this section some popular input matching topologies for an LNA will be considered. Also, their pros and cons and alternative solution will be considered. The simplest way of ensuring stable 50Ω matching at the input would probably be the use of resistive termination at the input (Fig 6.a) [4]. The biggest disadvantage of this topology would be the large detrimental effect on the LNA NF. This topology is known to increase the NF of the circuit by nearly two times. The noise mechanisms which come into play in this situation will be primarily the thermal noise introduced by the resistor itself and, the attenuation it causes to the input RF signal. An alternative to this is to use the source or emitter of a common-gate or common-base stage as the input termination (See Fig 6.b) [5]. Although theoretically the topology promises good termination and noise performance, it does not hold for short channel devices in CMOS. The minimum possible NF for CMOS is,

$$F = 1 + \frac{\gamma}{\alpha} \geq \frac{5}{3} = 2.2\,dB \tag{2.15}$$

Here, γ is the coefficient of channel thermal noise, α is the ratio of device g_m and zero-bias drain conductance. For long-channel devices, γ=2/3 and α=1. The NF expression neglects both short-channel effects ($\alpha \leq 1$) and excess thermal noise due to hot electrons ($\gamma \geq 2/3$). Indeed, for short-channel MOS devices, γ can be >>1, and α can be <<1. Accordingly, the minimum theoretically achievable noise figures tend to be around 3 dB or greater in practice.

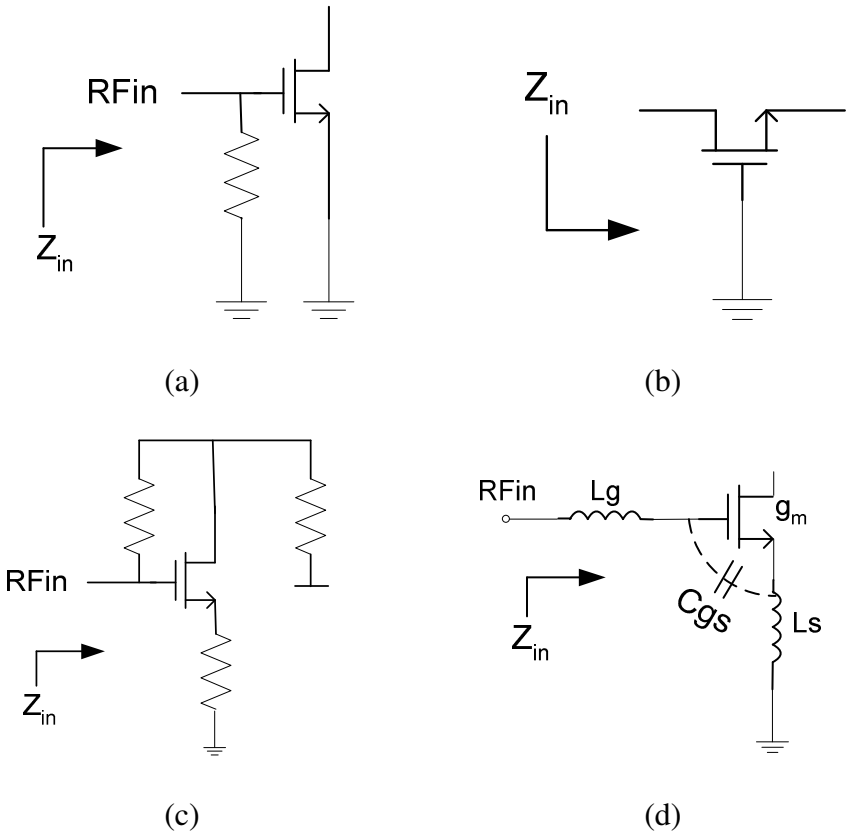


Figure 6. Input matching topologies for LNA

A further alternative is to use a series-shunt feedback method for setting input as well as output impedances [5]. However, this typical broadband architecture is prone to very high power dissipation compared to others with similar NF values. Depending on the application, the broadband performance may not be a requirement, especially if the target application is for single standards like CDMA or GSM. Also, high quality on-chip resistors may be the bottleneck in CMOS technologies. The final topology discussed is the inductive source degeneration method to eliminate the imaginary terms in the input impedance expression, leaving us with a purely real 50Ω input impedance [5]. This is the technique used in the LNA designed by the author and design details will be dealt with in Chapter 4.

For a source degenerated CMOS transistor, (See Fig 6.d), the expression for the input impedance can be deduced using the noise equivalent circuit. Looking into the gate of the active device, we can deduce the expression for Z_{in} as,

$$Z_{in} = s(L_g + L_s) + \frac{1}{sC_{gs}} + \frac{g_m}{C_{gs}} L_s \tag{2.16}$$

At resonance, the input impedance Z_{in} will be, $\omega_T Ls$, which is a purely real input impedance and can be designed to be 50Ω by choosing an appropriate value for the degeneration inductor *Ls*. The total noise factor, F, of the circuit has been deduced in [5] as,

$$F = 1 + \frac{R_l}{R_s} + \frac{R_g}{R_s} + \gamma g_{d0} R_s \left(\frac{\omega_0}{\omega_T} \right)^2 \tag{2.17}$$

From (2.17), it can be seen that the total noise figure of the topology can be reduced by reducing the g_{d0}, indicating a reduction in current, which ultimately leads to reduced power consumption. This is in contrast with the thermal noise expression (2.18), where the noise power, expressed by gate noise current i_{ng}, is inversely proportional to g_{d0} of the device and hence can be reduced by increasing the current and hence, the power consumption.

$$\bar{i}_{ng}^2 = \frac{4KT\omega^2 C_{gs}^2 \Delta f}{5 g_{d0}} \tag{2.18}$$

Thus, the inductive source degeneration topology has the much desired advantages of stable input impedance matching with NF optimization. Also, this topology is good for increasing the linearity of the circuit.

2.2.3 Gain and linearity

Although the source degeneration topology is used frequently for input matching stability and improving the linearity, it involves an important tradeoff with respect to the gain of the LNA and this will be discussed in the LNA design section of Chapter 4.

CHAPTER THREE

GAIN CONTROL IN LNAs AND ACTIVE BALUNS

3.1 Gain control in low noise amplifiers

As explained in the previous sections, the need for reconfigurability in today's state-of-the-art receivers is tremendous. One of the reconfigurability features for a receiver is the gain. Due to the presence of fading phenomenon resulting in signal power variation at the receiver front-end, gain controllability is needed to avoid saturation of receiver components and also aids in enhancing battery lifetime of handheld devices with its option of operating in the low-gain low-power mode.

Several gain control techniques have been presented before in the literature. Fig. 7(a) shows the traditional load switching technique [6], whose main advantage is that the circuit noise figure is not affected severely by the gain modes. However, the gain step in this case is very sensitive to parasitic impedance in the load chain and it may potentially pose voltage bias problems. Fig. 7(b) shows another technique which uses a bypass switch [7], to go around the active device and thereby achieve different gain levels. But in this circuit the switch path may actually induce losses. As long as the loss can be acceptable, this technique is usable. However, the gain and linearity are not controllable parameters. It is vital for reconfigurable systems to have precise control over the different configurations in which the circuit can be operated, in order to maintain expected behavior.

Next, the current splitting technique is considered (Fig 7.c) [8], where the gain step is dependent on the width ratios of M1, M2 and M3. Circuit gain is controlled by selective operation of the current control switches Vctrl1 and Vctrl2. The impedance seen at the RF input varies with the switching on or off of the control switches owing to additional impedance of the

transistors M2 and M3. Output matching may also cause problems for the same reason. However, the gain can be precisely controlled.

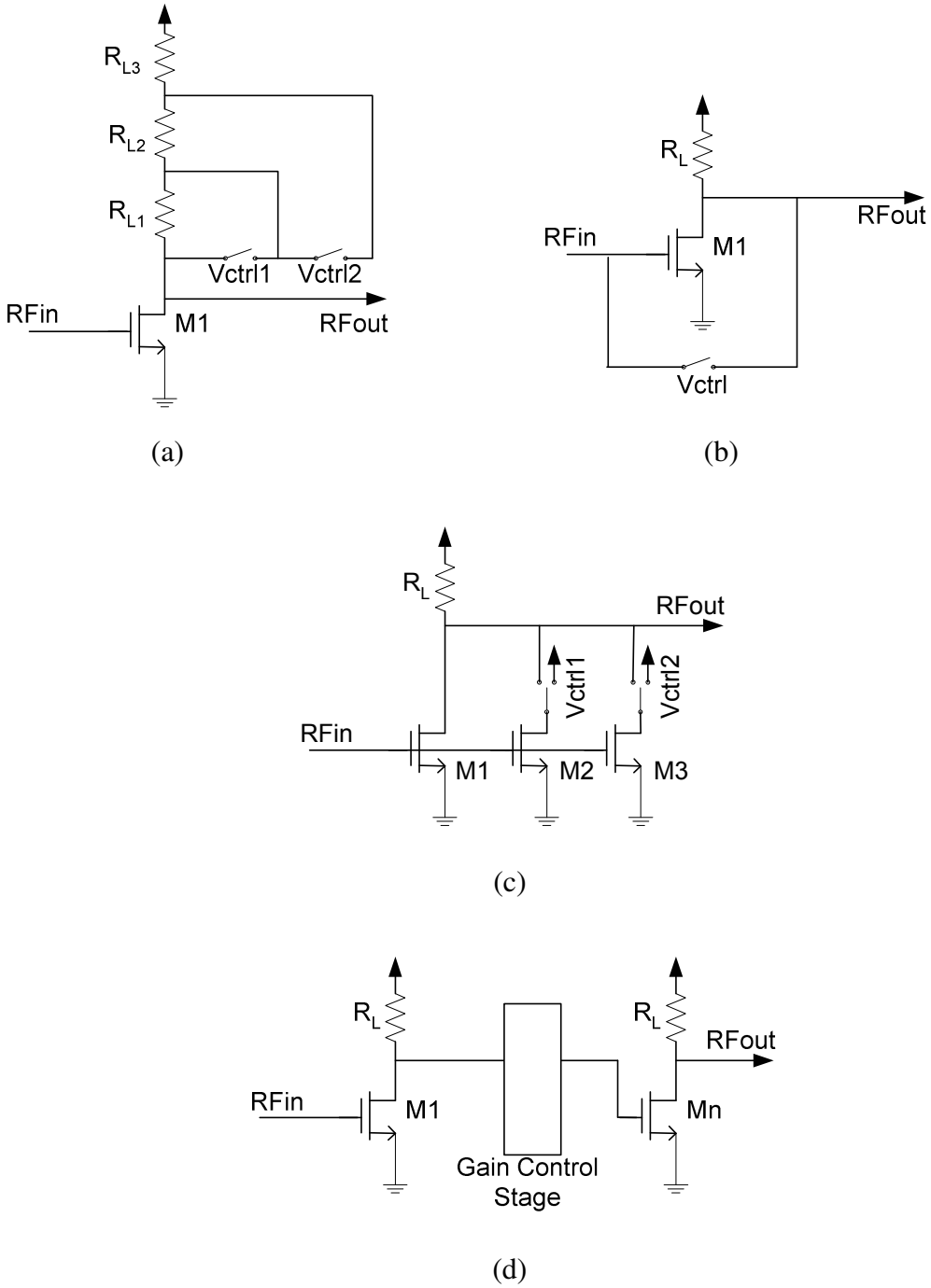


Figure 7. Gain control techniques (a) Load switching (b) Bypass switching (c) Current splitting (d) Gain control stage.

In the low gain modes, the noise is considerably degraded due to the presence of transconductance transistors M1, M2 and M3. Also, power consumption remains the same in both the modes because extra current, in the low gain modes, is dumped to the supply, which means power wastage. Fig. 7(d) shows one of the more recent methods of gain control [9], which utilizes an extra stage for varying the gain. The biggest advantage of this topology is the isolation it provides to the input and output matching networks from the different gain modes. But this advantage comes at the cost of silicon real estate. Additional stages mean larger die areas and large dies are not economically useful.

3.2 Active Balun: Needs and Requirements

Balanced and symmetrical design in RF circuits is preferred to an unbalanced one owing to its higher insensitivity to substrate and other noise sources. However, since an incoming RF signal is an unbalanced one, it is often desirable to split this into two differential signals, opposite in phase and equal in amplitude, and hence the need for baluns.

Current state of the art RF technology demands high performance baluns which are not lossy, do not induce noise into the signal and are silicon area efficient. It is very important to have balanced phase and amplitude between the differential signals in applications such as double balanced mixers where any imbalance can induce mismatches at the input port which cause intermodulation and dc offsets [10]. Well balanced signals help improve the second and third order intermodulation rejection for the mixer.

Several active balun topologies have been proposed in past and present literature [11-12]. The common source single-FET balun is probably the simplest (See Fig.8a) [11]. With the signal input to the gate, ideally the signal at the drain will be phase shifted by180 degrees relative to the signal at the source and have equal amplitude. However, this circuit becomes unsuitable for high frequency applications due to the presence of parasitics leading to uneven signal leakage to the

drain and source terminals. A common-gate topology cascaded with a common-source transistor can also be used as a phase splitter [12]. Again, high frequency performance limits the use of this topology. Also, the circuit uses capacitive coupling at the input and the second stage, making it a narrow-band solution.

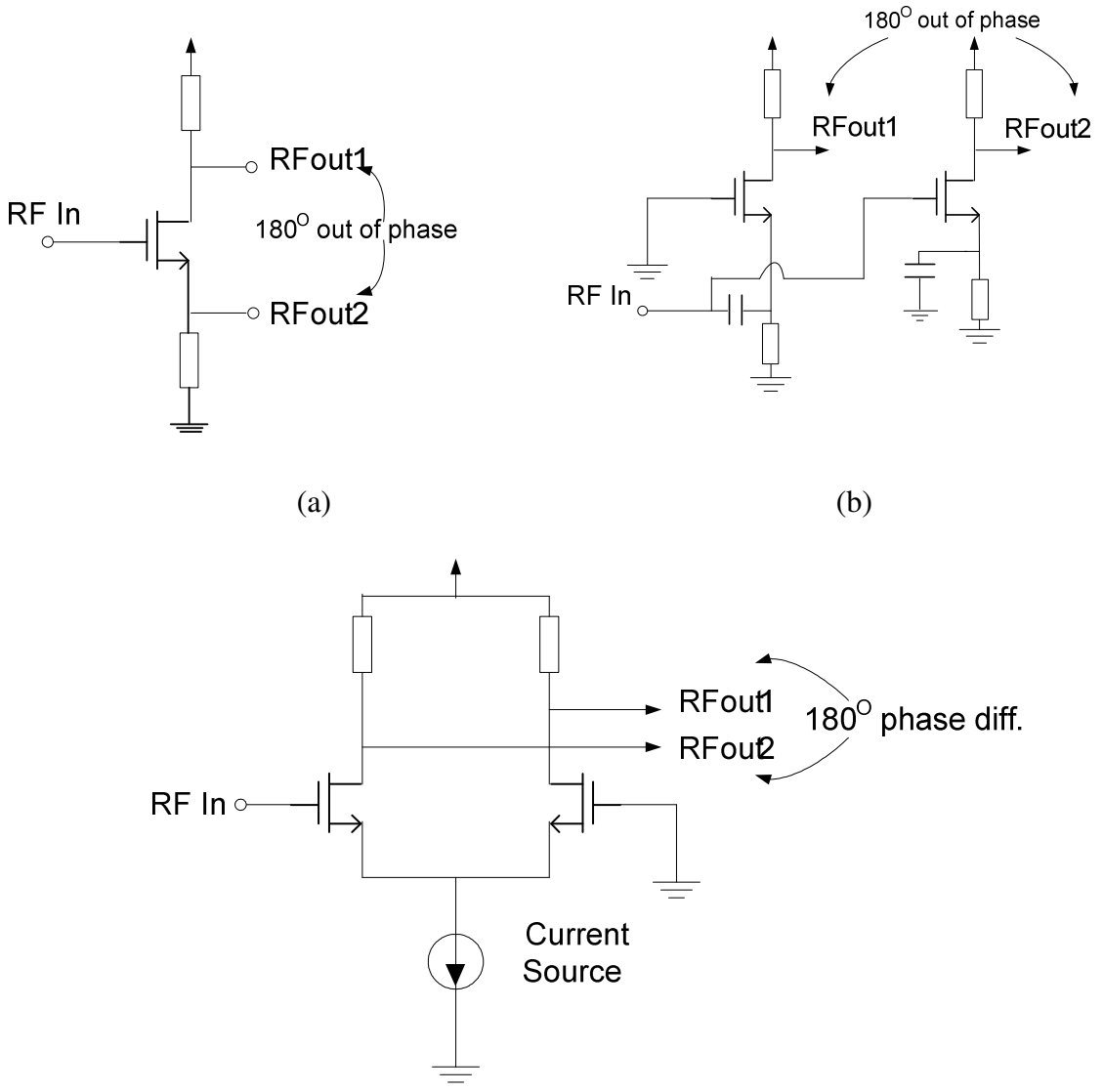


Figure 8. (a) Common source topology (b) Common gate cascaded with common source (c) Differential topology for active balun

A differential topology, (See Fig 8.c), is a strong candidate for use as an active balun, if conditions of operation are ideal. An RF signal applied at the input of one of the differential pair

transistors will ideally split equally between the pair thereby proving a 180^{O} phase shift between the two output signals. In other words, the gate-source potential for both the transistors, (See Fig.8), is equal and,

$$Vgs1 = Vgs2 = \frac{V_{RF}}{2} \tag{3.1}$$

However, the impedance of a non-ideal current source is not as high as required, resulting in unequal signal distribution, thereby leading to imbalance in the differential output. In order to have very high impedance at the base of the differential pair, Welch et al used an LC tank circuit resonating at the frequency of operation to create the desired effect of impedance (Fig 9) [13]. However, one major concern in this case would be that of resonance frequency. Unaccounted parasitics may be detrimental to the active balun operation leading to phase-gain mismatches. Careful layout is vital and can be quite challenging for a narrowband requirement.

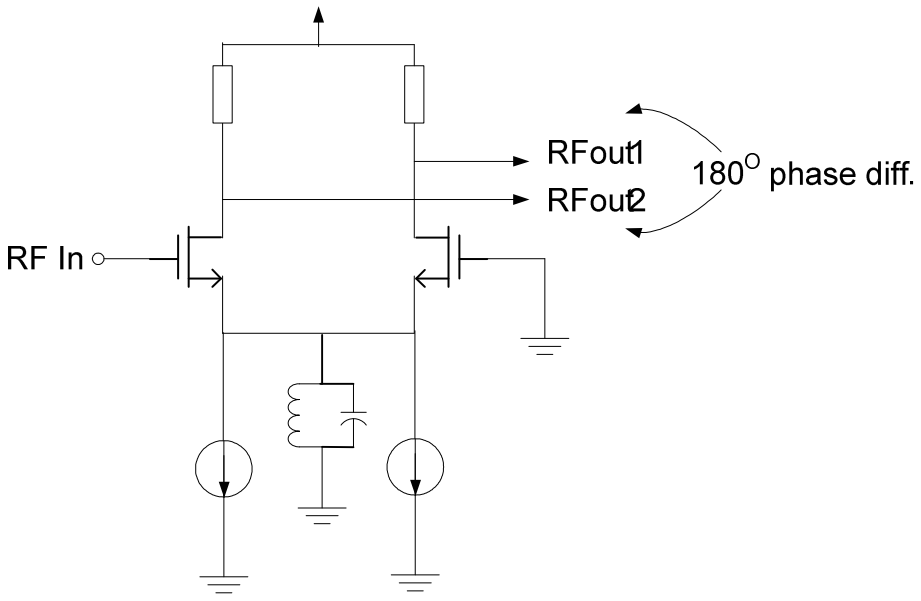


Figure 9. LC resonance to increase tail impedance

Another method of removing the imbalance due to low impedance at the tail is by feeding back a fraction of the single-ended input signal to the second input transistor [14]. This is the

method that will be pursued in the proposed design and will be explained further in the next chapter.

3.3 Current design

For the current application i.e. the 5GHz DCR, there is no need for a broadband balun. A narrowband active balun with small bandwidth will suffice. Typical receiver designs follow the pattern of having single-ended LNAs followed by an integrated balun and mixer circuit. However, in the proposed design, the balun is integrated with the LNA. As explained in the following chapter, the LNA and the balun are connected through a DC blocking capacitor, which also acts as the inter-stage matching element. Thus, the balun is an independent circuit by itself and can be used in other applications as well. The primary motivation for doing this was to keep each section isolated to reduce design complications. Further, gain control was introduced in the active balun section of the circuit not add to the existing design challenges of the LNA and mixer circuits.

The following chapter will go through the designed LNA and active balun circuits with emphasis on design challenges and techniques involved.

CHAPTER FOUR

DESIGN OF DUAL GAIN LNA WITH ON-CHIP ACTIVE BALUN

4.1 DGLNA Stage one

The first stage of the DGLNA is a conventional cascode structure with common source amplifiers and has an inductive load (See Fig. 11). The cascode structure has the advantages of high operating frequency and good stability because of the isolation provided by M2 between the input and output of the first stage and avoids Miller amplification of the gate-drain capacitance of M1. Also, a common source structure is inherently more suitable to achieve lower noise figures. However, non-optimized device size for the cascode stage could add at least 40% more noise power to the first stage [15]. Also, isolation decreases with larger device size of M2. Hence device width was optimized for low noise figure while maintaining sufficient isolation. As explained in 2.2.2, the input impedance for a source degenerated transistor amplifier is given by,

$$Z_{in} = s(L_s + L_g) + \frac{1}{sC_{gs}} + \left(\frac{g_{m1}}{C_{gs}}\right)L_s \tag{4.1}$$

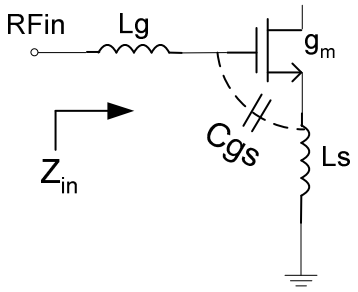


Figure 10. Input matching technique using source degeneration

The input network is reproduced in Fig 10 for convenience. By resonating out the gate-source capacitance, C_{gs}, using the source inductor, the input impedance can be made purely real. Thus, by proper choice of the inductors, L_g and L_s, it is possible to provide real 50 Ω impedance looking into the LNA. It also is one of the important contributors to achieving a low noise figure

and aids in noise matching by shifting the input impedance to an optimum point between Γ_{OPT} and G_{OPT}. Further, the noise figure is given by the noise parameters as,

$$F = F_{\min} + \frac{\left[(Gs - Gopt)^2 + (Bs - Bopt)^2\right]Rn}{Gs} \tag{4.2}$$

where, F_{min} is the minimum noise factor, Gs and Bs are the real and imaginary parts of source admittance Y_s, G_{OPT} and B_{OPT} are the real and imaginary parts of optimum source admittance $Yopt$ and Rn in the equivalent noise resistance. For noise figure to equal F_{min}, the source admittance has to be at or near the optimum admittance. Any offset in Ys and $Yopt$ is further amplified by Rn and degrades the NF. It also includes a tradeoff with the best matching point at the input. Hence, to improve the NF, the input matching has to be traded in this design. The inter-stage matching between the first and the second stages of the DGLNA is dictated by the coupling capacitor Cc, the load inductance of the first stage and the gate-drain parasitic capacitance of the cascode transistor.

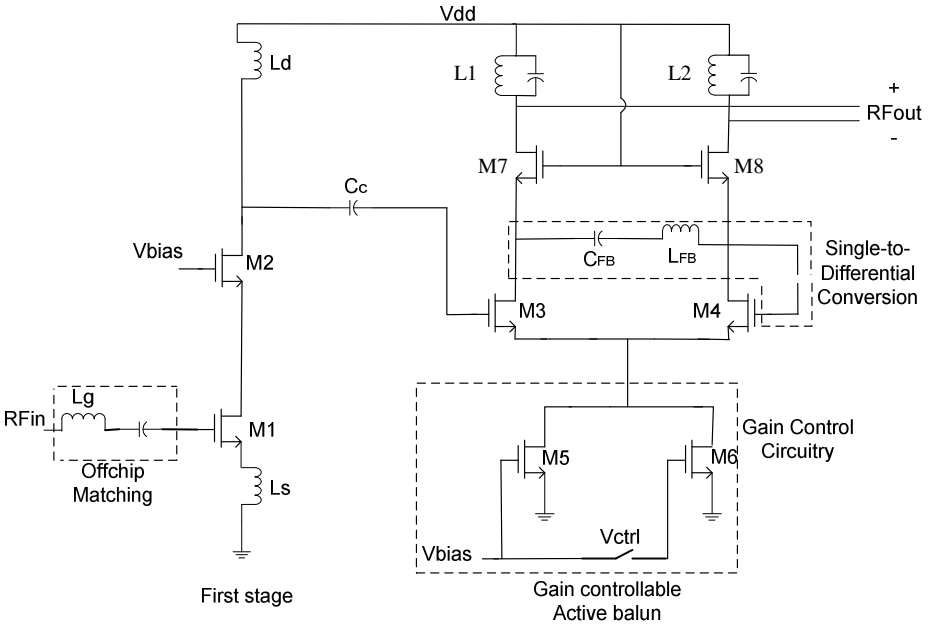


Figure 11. DGLNA with gain controllable active balun (DC bias not shown)

Another important trade off involved in this design is that of gain versus linearity as was mentioned in 2.2.2. Using the small signal model, we can deduce the equation for the transconductance as,

$$Gm = \frac{g_m}{1 + \left(g_m + g_{mb} + g_o\right)Rs}, \tag{4.3}$$

and it turns out to be a ratio of linear passive element values for large *Rs* value. Thus, the result is that the linearity of the LNA is controlled by the passive elements, namely the source degeneration resistance. However, the value of the transconductance is now reduced by a factor dependent on the source degeneration value. Thus, increasing the source degeneration resistance increases linearity, but reduces the gain. In low-voltage designs, the head room is small. Thus, using a resistor for source degeneration would further limit the swing and hence is not used. Instead, an on-chip or off-chip inductor is utilized for the same purpose and it also has the advantage of input matching, as was explained earlier.

4.2 On-Chip Active Balun

We discussed in 3.2 the issues associated with active baluns and how the differential topology can be utilized for effective phase splitting. Due to the absence of very high impedance at the tail of the differential pair, signal splitting is not exactly even and hence leads to phase and gain mismatches. In order to overcome the unequal signal distribution in a differential topology, a fraction of the input signal can be capacitively coupled to the second input transistor [14]. Capacitive coupling is necessary for DC isolation between the two transistors (See Fig.11). A series inductor is added in the signal path to nullify the phase shift provided by the capacitor. Also the series LC circuit, when resonaing at the frequency of operation, provides a low impedance path for the coupled fraction of input signal. The value of the inductor is calculated using (4.4) to form the series LC circuit that resonates in the desired frequency range.

$$L_{FB} = \frac{1}{\omega^2 C_{FB}} \tag{4.4}$$

A cascode topology is used in order to isolate the active balun circuit from variations in the load and to isolate the output matching network from DC bias point variations in the circuit. This also contributes in improving the intermodulation immunity of the receiver by reducing the static DC offset in a direct conversion receiver (DCR). Also, device mismatch, which is a primary cause of DC offsets in a DCR, was reduced by using a fully differential approach and a symmetric and balanced layout.

4.3 Gain Controllability

The gain of the DGLNA is primarily controlled by selectively operating the current sources. A control voltage, V_{Ctrl}, is used to turn one of the current sources on or off, thereby controlling the DC gain of the balun. This effectively overcomes the dynamic signal amplitude issues at the front end of the receiver. Since S-parameters are a function of the DC bias point of the circuit, care has been taken to see that adequate matching is available at the input and the output of the balun in both the high gain mode (HGM) and the low gain mode (LGM).

4.4 DGLNA Layout

The layout for the DGLNA was done using Cadence Virtuoso layout editor with the TSMC CMOS 0.25um design kit. Three different layouts were created as seen in Fig 12, 13 and 14. The first is the DGLNA layout with on-chip inductive loading, second is another version of the DGLNA which uses the bond-wire inductance as load for the first stage and finally, the third is the gain-controllable balun as a stand-alone circuit. Robust ground conditions were created using a vast ground plane.

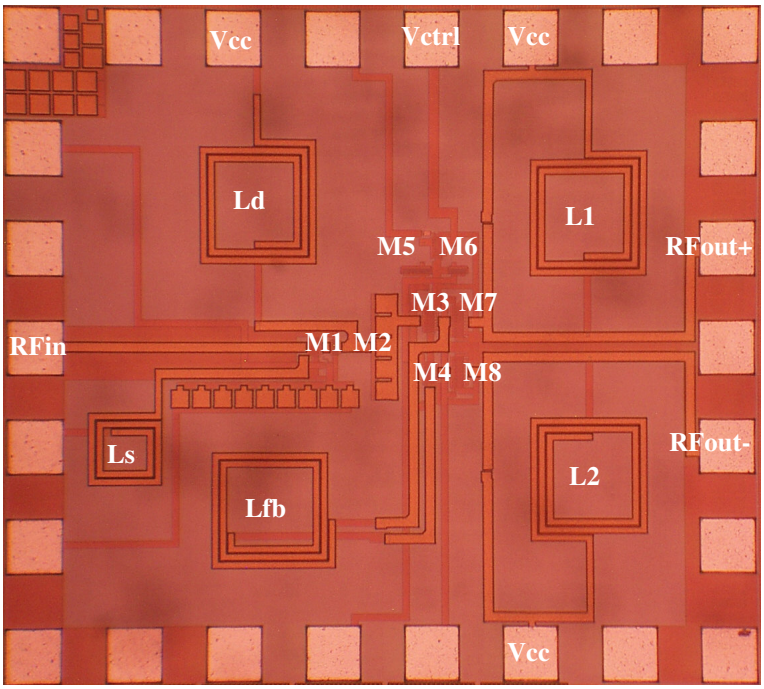


Figure 12. DGLNA layout micrograph

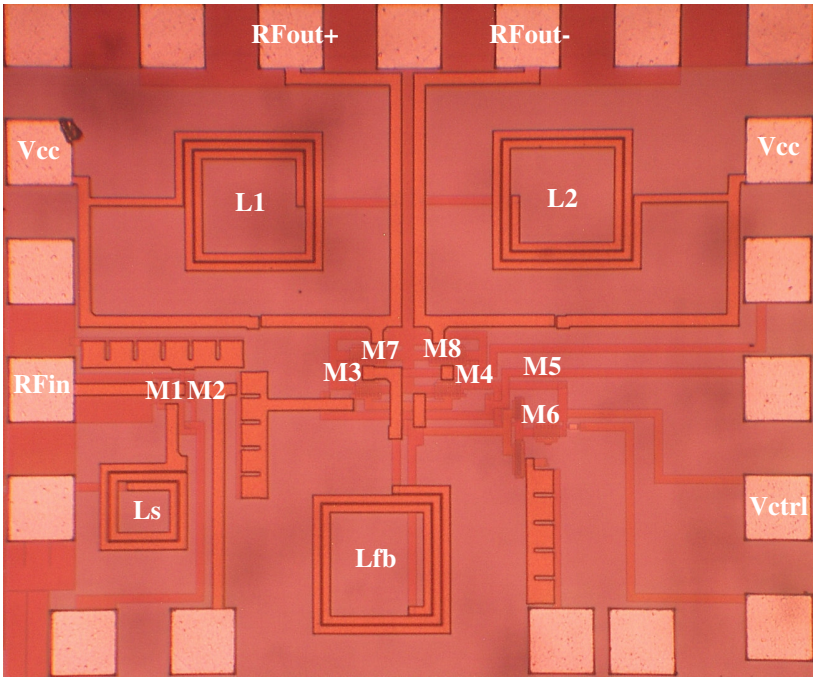


Figure 13. DGLNA version 2 layout

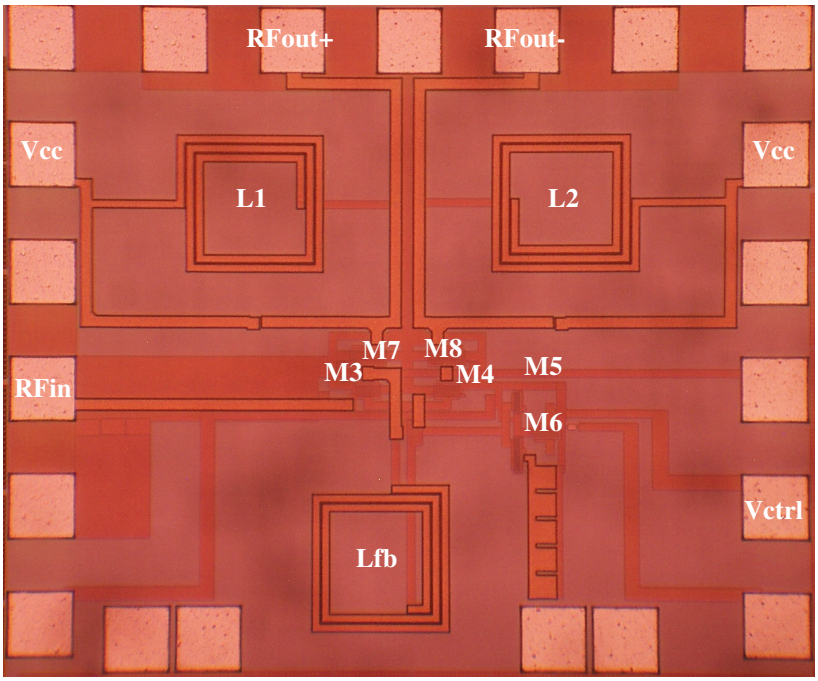


Figure 14. Gain controllable active balun layout

Chapter six will cover the measurement setup used for characterizing the DGLNA and the gain-controllable active balun and also the results obtained. It will be followed by a brief summary and conclusion.

CHAPTER FIVE

LINEARITY ENHANCEMENT IN LNAs

5.1 Linearity phenomenon in CMOS LNAs

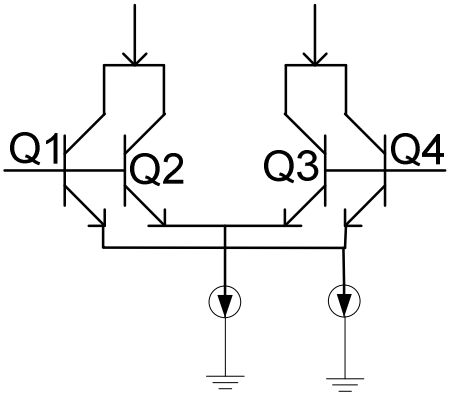
The focus in the previous LNA design was primarily on the gain control and active balun performance. The trend for reconfigurable front-end components drove the previous design and hence the multi-gain feature and active balun topologies. Consequently the design was not optimized for high linearity performance. However, linearity of an LNA is a very important parameter as was explained in chapter 2. The two major sources of non-linearity for a CMOS LNA are the transconductance and output conductance non-linearity. Up to frequencies of about 4GHz, the output conductance non-linearity is dominant, while at frequencies above that, transconductance non-linearity becomes dominant [16]. Keeping this in mind, for an LNA with target frequency range of 5-6GHz, steps to counter the transconductance non-linearity will be of primary interest.

5.2 Linearity enhancement techniques

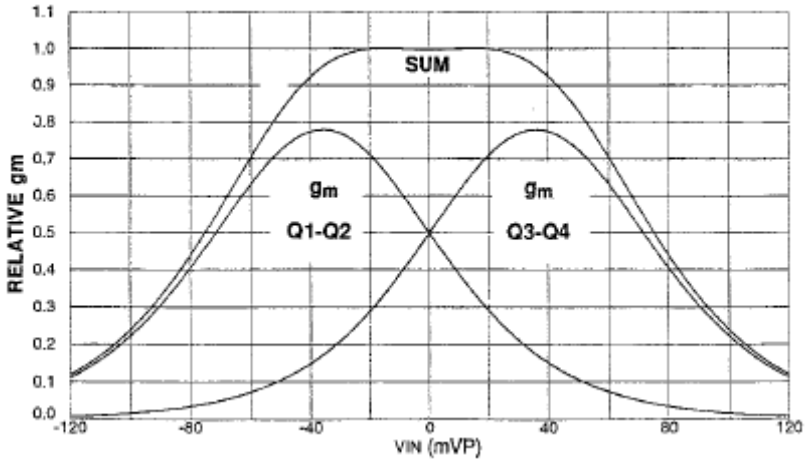
There are several methods proposed in the literature to improve an LNA's linearity or third or inter-modulation performance. We shall cover a few of them here and look at their pros and cons and then introduce the proposed method.

One is the use of a multi-tanh topology, which is popular in the BJT domain (Fig.15) [17]. The basic principle involved in this technique is illustrated in Fig. 15. By superposition of the offset gm characteristics, using either voltage offset or current offset, the resultant gm characteristic can be made such that it is linear over a wider range if input voltages, as seen in the figure. This principle can be extended further to include the transistor pairs or more to further

increase the linear region area. It should be noted however, that the area under the g_m(Vin) curve remains constant, irrespective of the change in shape.



(a)



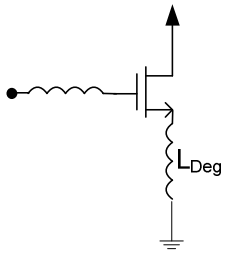
(b)

Figure 15. Multi-tanh technique to improve the IIP3 of a circuit (a) Circuit topology (b) g_m characteristics

The additional stages for multi-tanh topology are, however, detrimental to the noise figure of the circuit. A similar technique is present for the CMOS domain, although it targets the third order transconductance of the devices rather than the first. This technique, called the gm3 cancellation technique will be explained in the following sections. Another major issue related with this method is the increased power consumption. For state-of-the-art DCR solutions, the low power

consumption is an important requirement and hence the multi-tanh principle is not very promising.

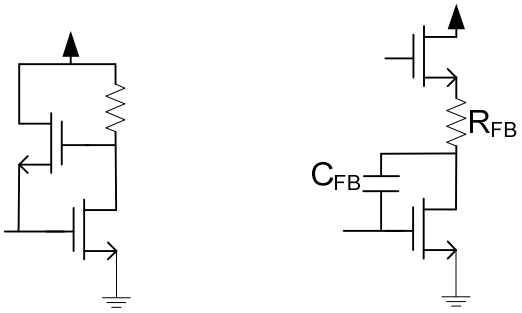
Next, discuss a simple, but moderately effective method to improve the linearity, which utilizes source degeneration. As seen in Fig.16, the topology consists of a source degenerated transistor, whose gm characteristics reduce to a linear ratio of source and drain loads. This linear ratio is what forms the core of this method. All intricacies and trade-offs involved with source degeneration were explained in chapter 4.



$$gm = linear\ ratio \propto \frac{1}{R_{DEG}}$$

Figure 16. Inductive source degeneration for IIP3 improvement

Active and passive feedback is another useful method for improving the linearity of an LNA (See Fig.17). The enhancement in linearity due to feedback topologies is not significant. Also, passive feedback can be detrimental to noise and also may pose circuit stability issues due the presence of uncontrolled feedback.



(a) (b)

Figure 17. Feedback topologies (a) Active feedback (b) Passive feedback

Active feedback on the other hand provides controllable feedback and aids in reducing harmonic feedback in the gate-drain region, thus resulting in reduced third order intermodulation. However, the improvement is balanced by increased noise at the input and increased power consumption.

5.3 g_{m3} cancellation technique

An effective method of reducing third order intermodulation is to cancel the third order transconductance (g_{m3}). The drain current of a common source FET can be expressed by the Taylor series as,

$$i_{DS} = I_{dc} + g_m v_{gs} + \frac{g_{m2}}{2!} v_{gs}^2 + \frac{g_{m3}}{3!} v_{gs}^3 \tag{5.1}$$

Here, v_{gs} is the small signal gate-to-source voltage and g_m is the n_{th} order transconductance. The third order transconductance g_{m3} plays a very important role in the linearity of a device. A plot of g_{m3} (See Fig.18) shows a negative peak in the voltage range of 0.5V to 0.9V , which is the desired operating gate voltage to achieve optimum power consumption with good matching and noise figure. Using the transconductance of an additional parallel transistor, M2, operating in the triode region, this negative peak can be compensated for (See Fig. 18). This effectively leads to improved IIP3 and hence, linearity. But again increased power consumption is an issue with an additional current path. To keep the power consumption low while using an additional transistor, this secondary transistor can to be operated in the sub-threshold region.

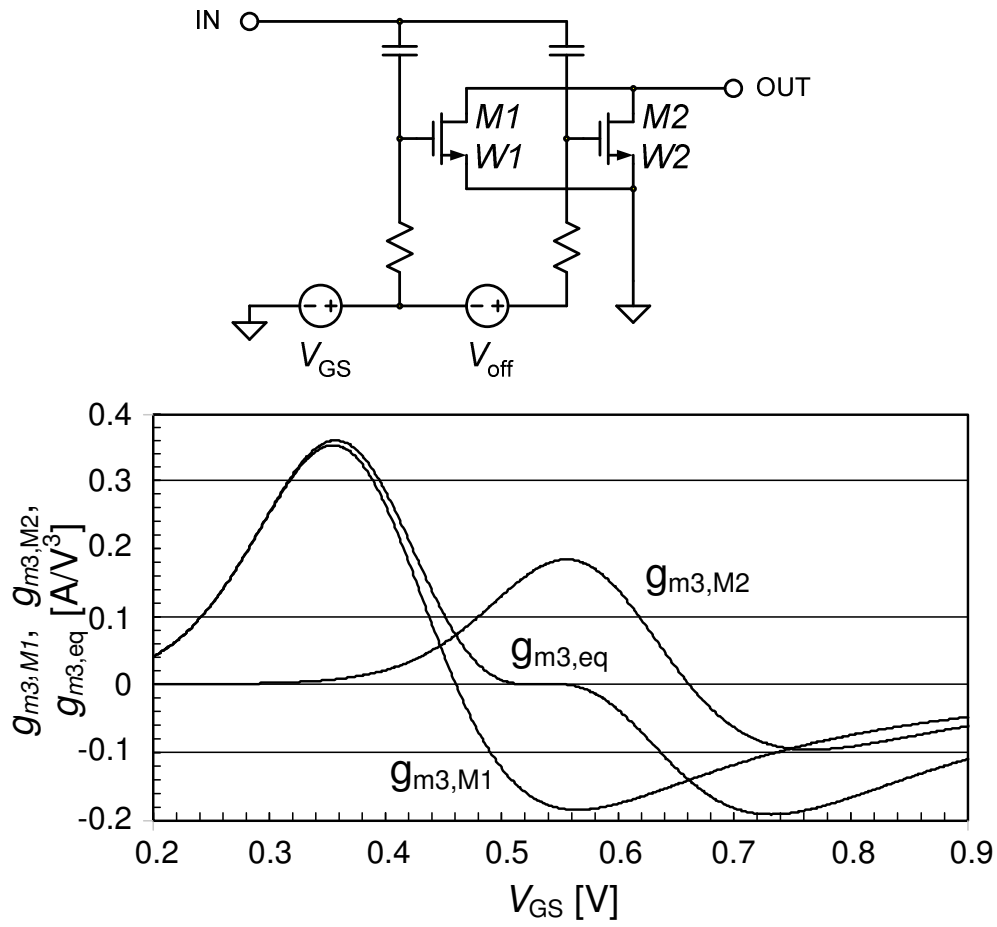


Figure 18. Illustration of gm3 cancellation technique

Although the gm3 cancellation technique works well in theory, in practice there are several issues involved. Earlier designs have all used negative feedback, in the form of a degeneration inductor, for linearization in addition to nonlinearity cancellation [18]. The major drawback associated with this technique is the contribution of second order nonlinearity to the IMD3. The source degeneration inductance creates a feedback path for the drain current to the gate-source voltage, v_{gs}. This feedback is particularly strong for high frequency spectral components of the drain current [18]. For example, the 2nd harmonics generated by $g^2v^2_{gs}$ are fed back across the gate and source adding to the fundamental components of v_{gs}. These spectral components are then mixed in $g^2v^2_{gs}$ to produce the responses at $2\omega1\pm\omega2$ and $2\omega2\pm\omega1$. Thus, use of a

degeneration inductor introduces unwanted spectral components leading to degradation of system linearity.

In order to overcome the mentioned issues, we introduce the use of shunt feedback instead of series feedback, as in the case of a degeneration inductor. Thereby, the advantages of negative feedback to reduce the harmonic feedback are retained, while the contribution of second order nonlinearities to the overall IMD3 is reduced considerably. Further, unlike series feedback which increases the impedance at the input gate of M1, shunt feedback does not [19]. This effectively translates to a lower noise contribution. Active feedback is an option that can be pursued, but the downside is the increase in power consumption due to additional current in the feedback path [20]. Fig.19 shows the proposed architecture for the Enhanced Linearity Low Noise Amplifier (EL^{2}NA).

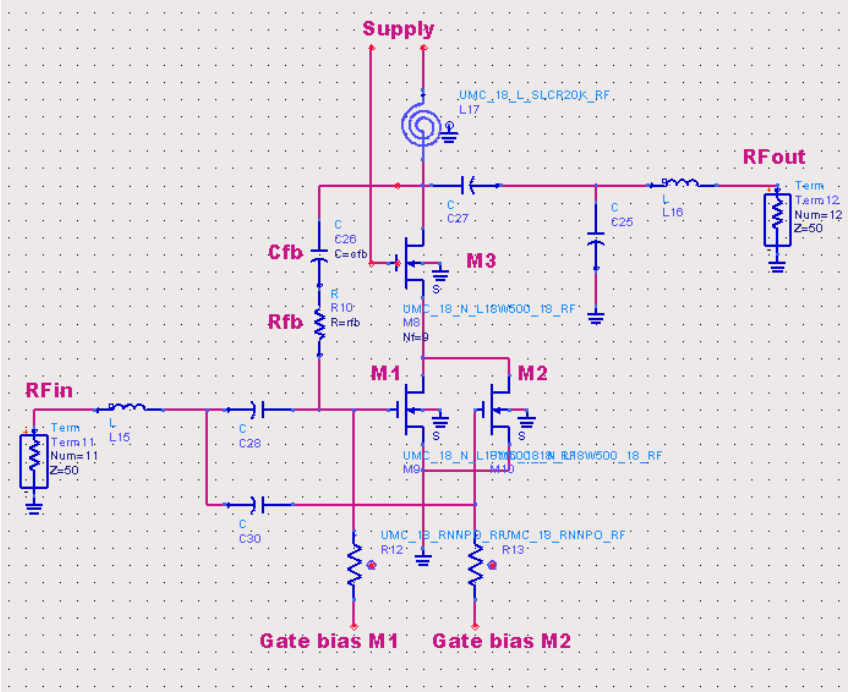
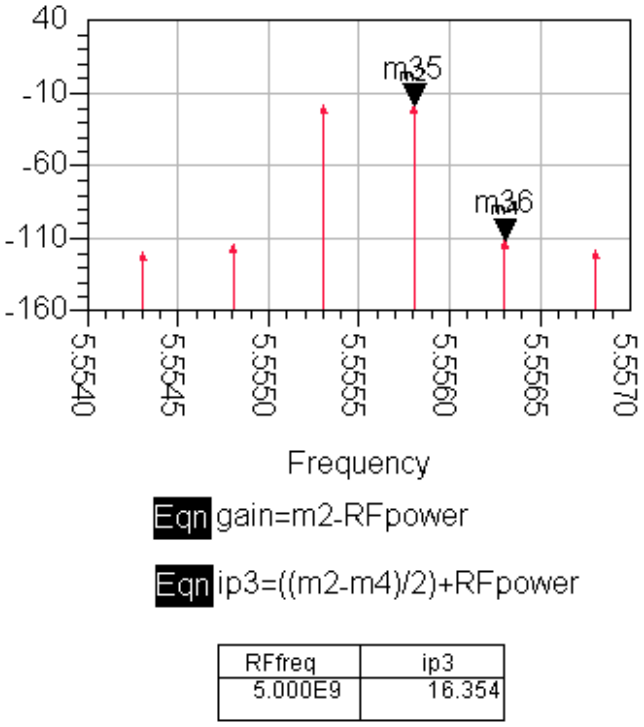


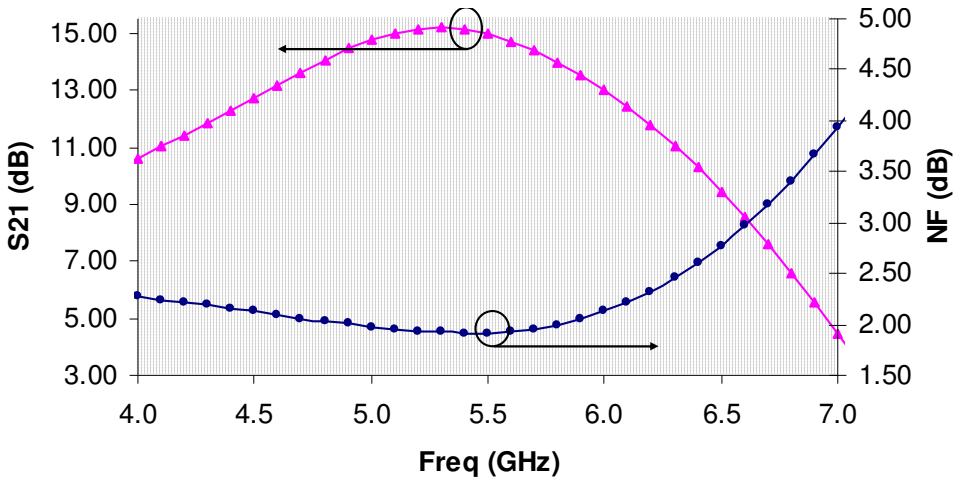
Figure 19. Enhanced linearity LNA (EL^{2}NA)

Simulation results show an IIP3 of +20dBm with 9mA of current drawn from a 1.8V supply while providing a gain of 15dB. This is one of the best linearity performances in the

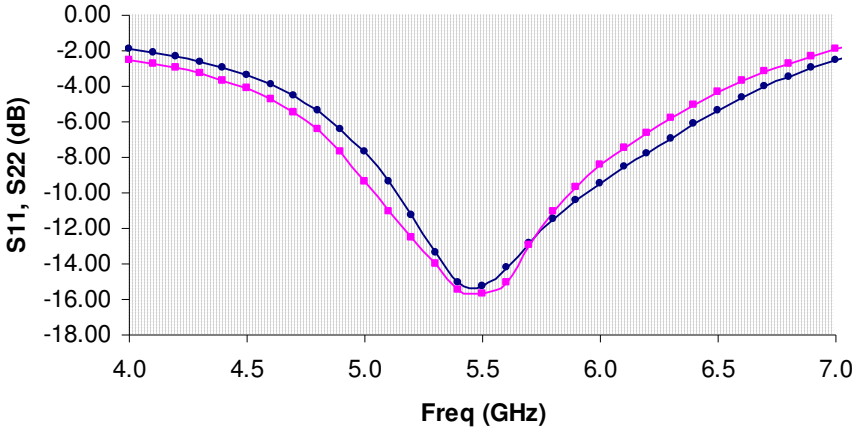
5GHz range. Input and output reflection coefficients are shown in Fig.20 and are less than -15dB. The noise figure is below 2dB, and it needs to be mentioned here that the g_{m3} cancellation topology inherently has a higher noise contribution [18]. The use of the enhanced g_{m3} cancellation technique gives an improvement of at least 10dBm over conventional methods of IIP3 improvement. All simulation results are shown in Fig.20.



(a) IIP3



(b) S21 and NF



(c) S11 and S22

Figure 20. Simulation results for EL^{2}NA

The proposed LNA was designed using the 0.18um CMOS process from Jazz Semiconductor's SiGe BiCMOS technology. All simulations were carried out in Agilent's Advanced Design System (ADS) and layout was done in Cadence Virtuoso Layout editor. The silicon layout of the EL^{2}NA is shown in Fig 21. The total area of the LNA is less than 0.8mm^2, including the test pads.

The EL^{2}NA, when compared to the previously published high-linearity LNA structures in the 5GHz frequency range, has the best overall figure of merit (FOM). The FOM is defined as,

$$\text{FOM} = (\text{OIP3}) / [(\text{NF}-1)*(\text{power consumption})] \quad (5.2)$$

The state-of-the-art in 5GHz highly linear LNA designs is [21] and although it displays very good IIP3, the presence of multiple modules in the circuit, would probably lead to high power consumption. The LNA design has been submitted to the Jazz foundry for fabrication and silicon characterization will be carried out once the fabricated chip returns, to validate the simulation results. In order to aid in the silicon characterization process, the matching was implemented partly on-chip and partly off-chip. On the chip, multiple shunt capacitors have been added

instead of a single large one at the input and output. Depending on the matching requirements,

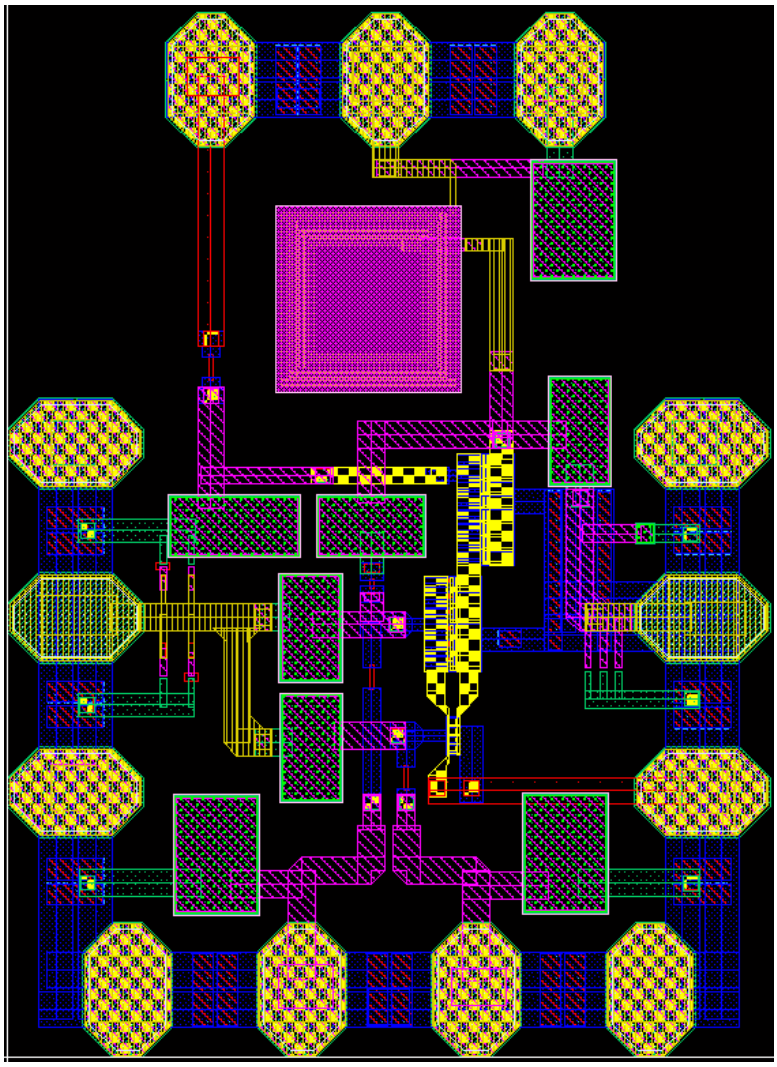


Figure 21. Enhanced Linearity LNA layout

one or more of the capacitors can be disconnected using a laser cutter, available at the Washington State University's ETRL B24 lab. This introduces a certain amount of flexibility has been introduced in the matching process while maintaining the advantages associated with on-chip passive components. The off-chip part of the matching networks provides a larger degree flexibility.

CHAPTER SIX

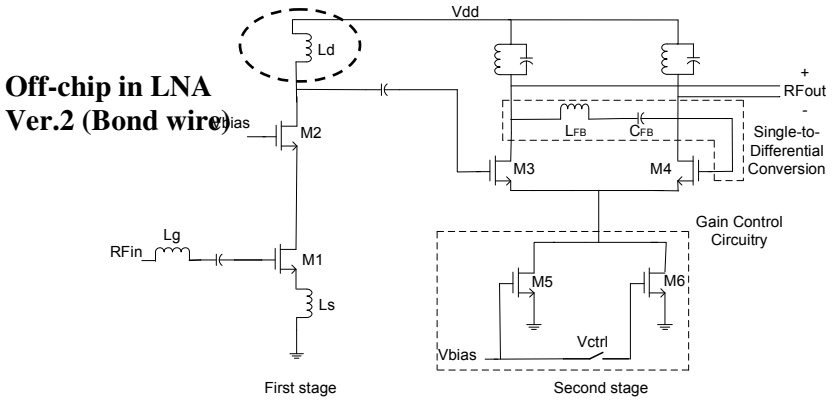
RESULTS AND CONCLUSION

6.1 Measurement Setup

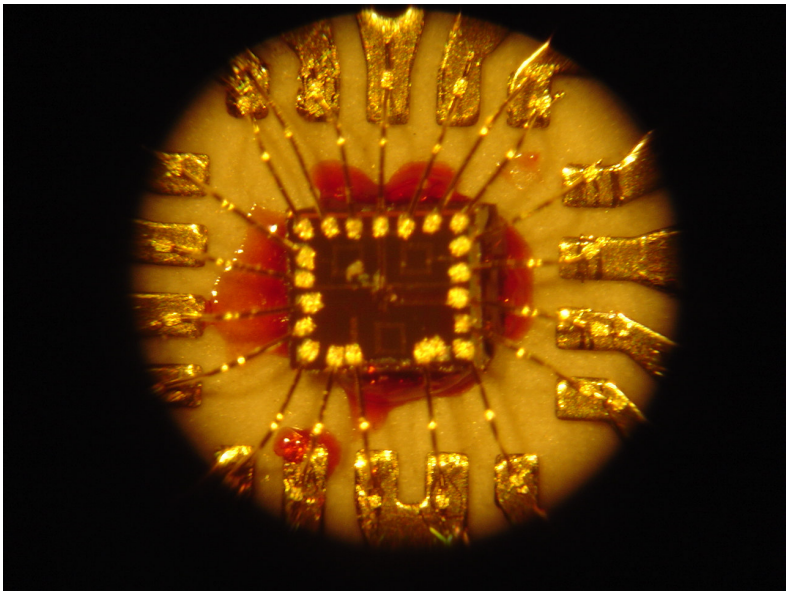
A 5.6 GHz low noise amplifier has been designed using an inexpensive, TSMC 0.25um CMOS process and characterization to validate simulation results was performed using evaluation boards as well as on-chip measurements. Fig.22 shows the measurement setup and the DGLNA architecture details for reference. The DGLNA was designed and simulated to operate in two gain modes and has an integrated gain controllable active balun. Simulations showed gains of 20dB and 12dB in the high and low gain modes, respectively, with an IIP3 of -11.5dBm and noise figure of 3.1dB. Unconditional stability was achieved in simulation environment with stability factor, $K > 1$. However, the measurement progress has been hampered by several factors to date. Since the dies were not in packaged form, the first challenge was overcoming electrostatic discharge issues at the wire-bonding stage, causing gate breakdowns. Gold wire was used for bonding the die to the evaluation board (see Fig. 22.b). Careful grounding of all metal surfaces and the test environment ensured safe usage of the dies. Further, all signal lines and DC paths were first bond-wired to adjacent ground plains, so that, any voltage surge seen on the RF and DC signal lines would be safely shorted out to ground. The next challenge faced during the measurement process of the LNA was that of random oscillations. Being an amplifier, any random oscillation is amplified to higher magnitudes, large enough to cause a gate or drain breakdown. Low frequency oscillations cannot be measured due to instrument limitations and hence of particular concern as they may lead to breakdown. To overcome this issue, filtering capacitors were used at all gates and drains, of the RF FETs. Particular attention was given to stopping oscillations on supply lines which may induce oscillations starting with low frequency oscillations. A large capacitor for low frequency shorting and a smaller capacitor for higher and

in-band oscillation reduction were used for the mentioned effect. Although these measures stabilized the test environment considerably, especially at the output, the input stage still suffers from oscillation issues. Current measurement results still show signs of oscillations and work is in progress to suppress oscillations further.

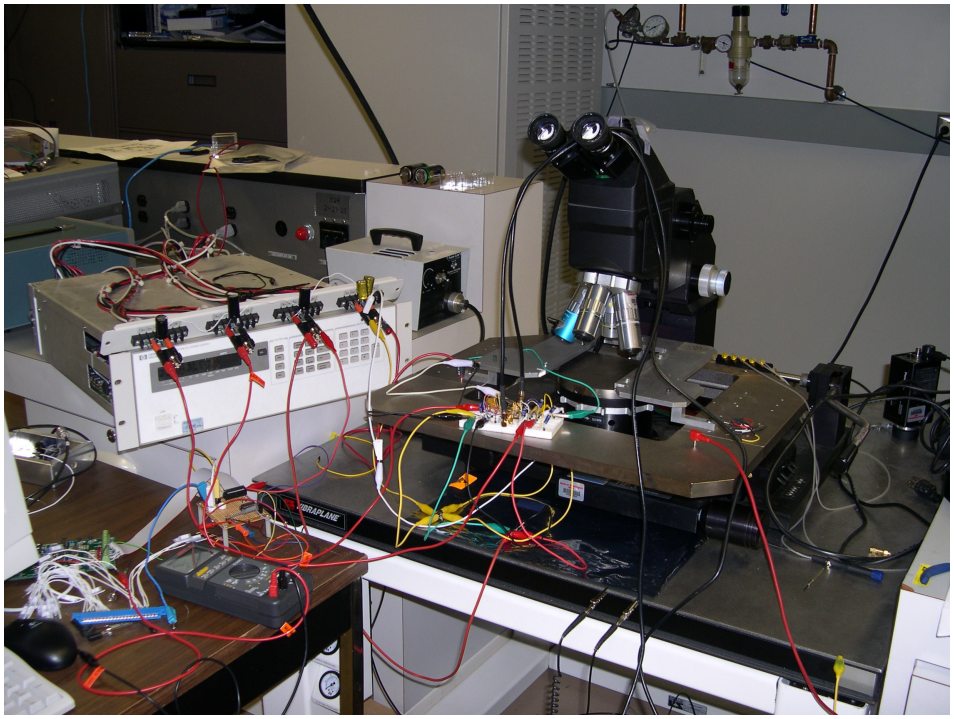
Two versions of the DGLNA were designed and simulated, with the second version using bond wire inductors in place of on-chip inductor load for the first stage. Separate measurements have been carried out on the on-chip active balun which was designed as a stand alone circuit using on-wafer probing (See Fig. 22(d)).



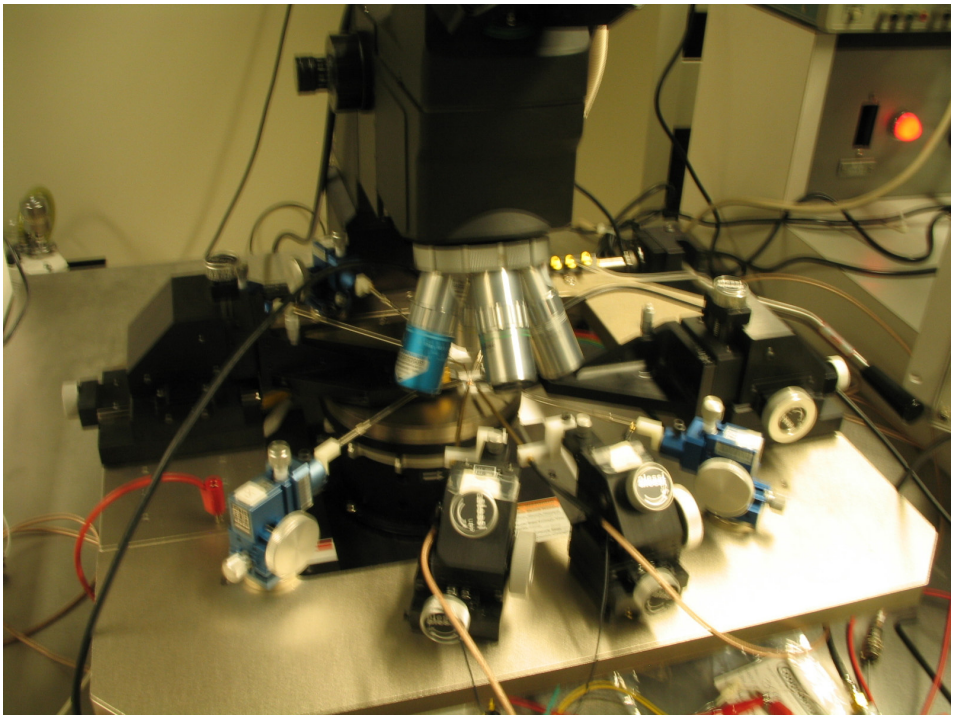
(a) DGLNA architecture



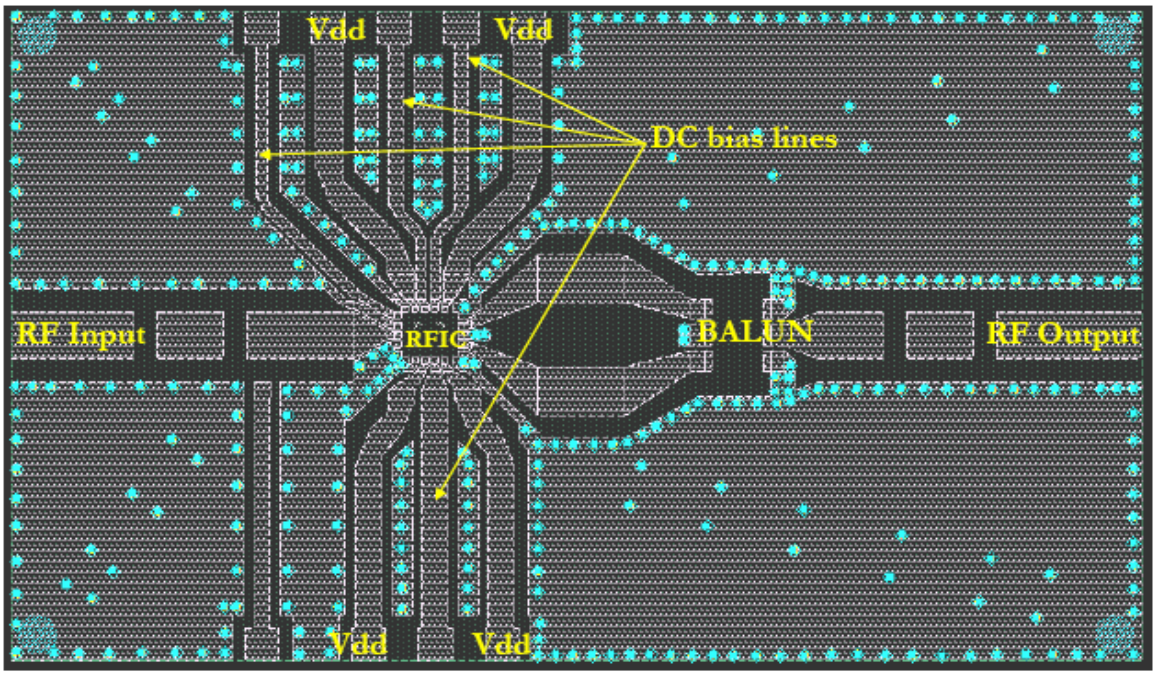
(b) Wire-bonded die



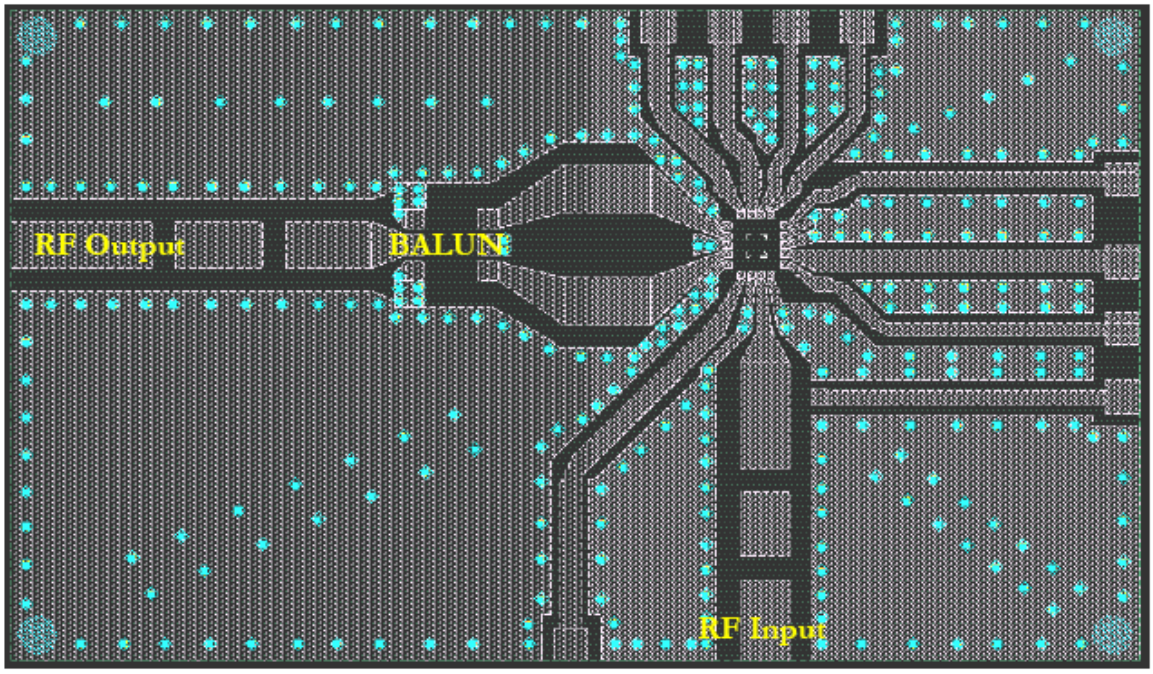
(c) DGLNA evaluation board test setup



(d) GCAB on-wafer probing setup



(e) Evaluation board for DGLNA Version 1



(f) Evaluation board for DGLNA Version 2 and GCAB

Figure 22. DGLNA and GCAB measurement setup details with designed evaluation boards

6.2 Simulation Results

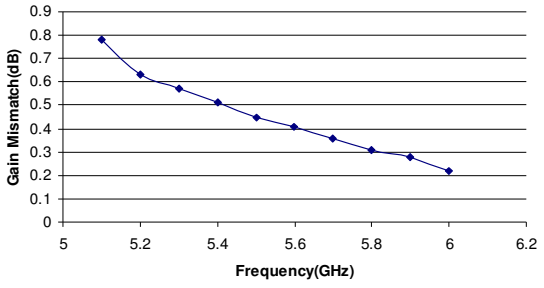
The active balun shows gain mismatch less than 0.5 dB and phase mismatch of about 1˚ over a 400 MHz bandwidth. Furthermore, there was no considerable degradation of performance due to mode switching. Fig. 23.d shows the gain plots for both the HGM and the LGM with gains of 19.5 dB and 12 dB in the two modes respectively. The DGLNA exhibits a NF of 3.1dB, which is good considering the fact that this includes the noise from the balun as well. The best IIP3 achieved was -11.5 dBm with 10mA of current from a 3V supply. Table I summarizes the results and Fig.23 shows the simulation plots.

TABLE II

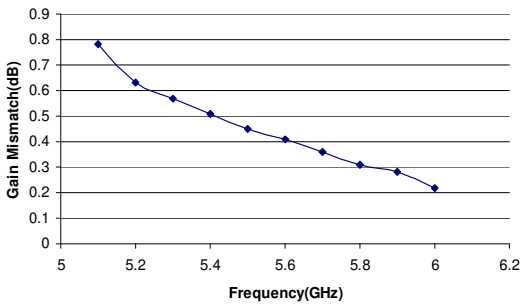
PERFORMANCE SUMMARY

Parameter	Value	
Mode of Operation	HGM	LGM
Frequency of Operation	5.6GHz	
Current from 3V supply	10mA	5mA
Gain Matching	< 0.5 dB	
Phase Matching	< 1 degree	
Gain	20 dB	12 dB
Noise Figure	3.1 dB	3.5 dB
IIP3	-11.5 dBm Best	
S11	< -5 dB	
S22	< -23 dB	
Isolation	< -60 dB	

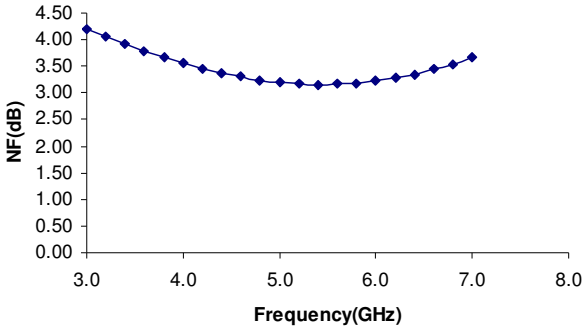
Fig. 22 shows a picture of the LNA and the wire-bonded die. Microstrip line technique was used to contain the electromagnetic field of the RF lines and improve isolation. The total size of the chip including the active balun is 1.1mm X 1 mm.



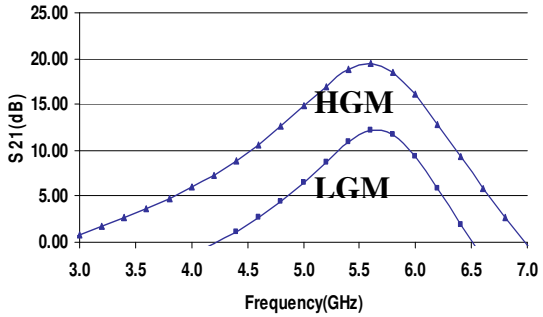
(a) Phase mismatch



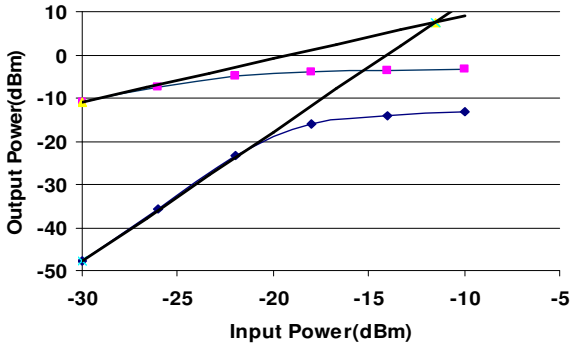
(b) Gain mismatch



(c) NF



(d) S21



(e) IIP3

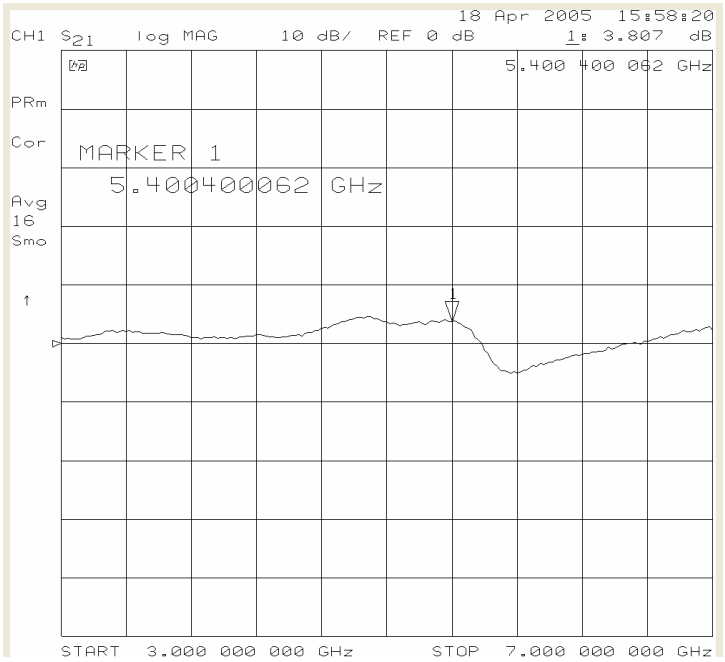
Figure 23. DGLNA and GCAB simulation results

6.3 Measurement results

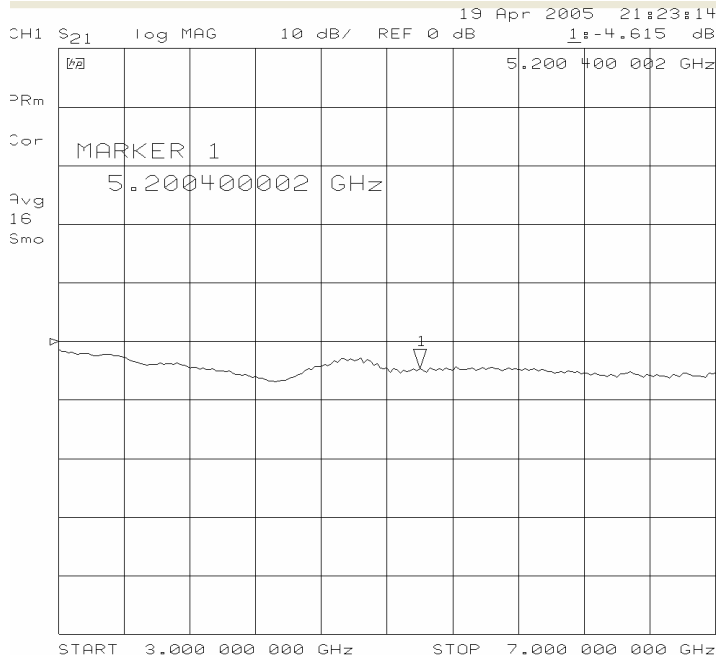
As was mentioned previously, LNA measurements are still showing signs of oscillations and hence good measurements are very challenging to make. Several efforts to rid of this were made and have been explained before. Efforts are in progress to get stable and clean results.

On-wafer probing was carried out on the GCAB and this meant, the circuit had to be measured without the input and output matching networks. However, as a proof of concept, the measurements were carried out and results are shown below. Firstly, the S-parameter measurements were carried out using an HP 8719D Network Analyzer. It can be seen from the S-parameter plots, that due to lack of matching, the results are fairly broadband. S21 values of 4 dB and -4.6 dB were achieved in the high and low gain modes of the GCAB at 5.4GHz. Shift in center frequency is primarily attributed to lack of narrow band matching at the input and output. Gain mode switching was done by turning on or off, the secondary current source, thereby

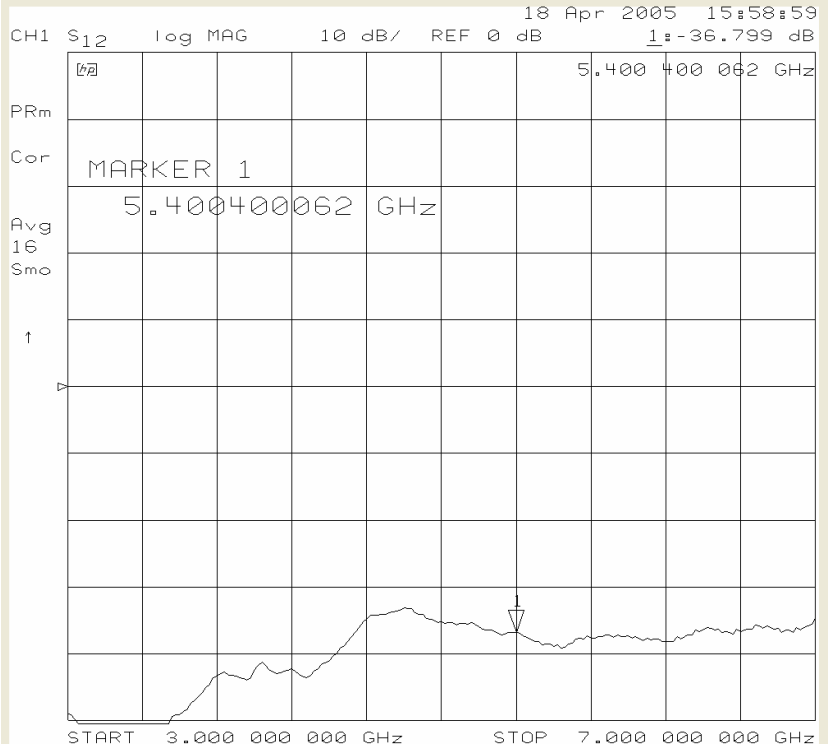
controlling the current in the circuit. Thus, a gain margin of about 8.5 dB was achieved. However, it should be noted here that with the use of input and output matching networks, the gain levels in both modes of operation can increase significantly and attempts are being done to do this by doing the measurements on an evaluation board.



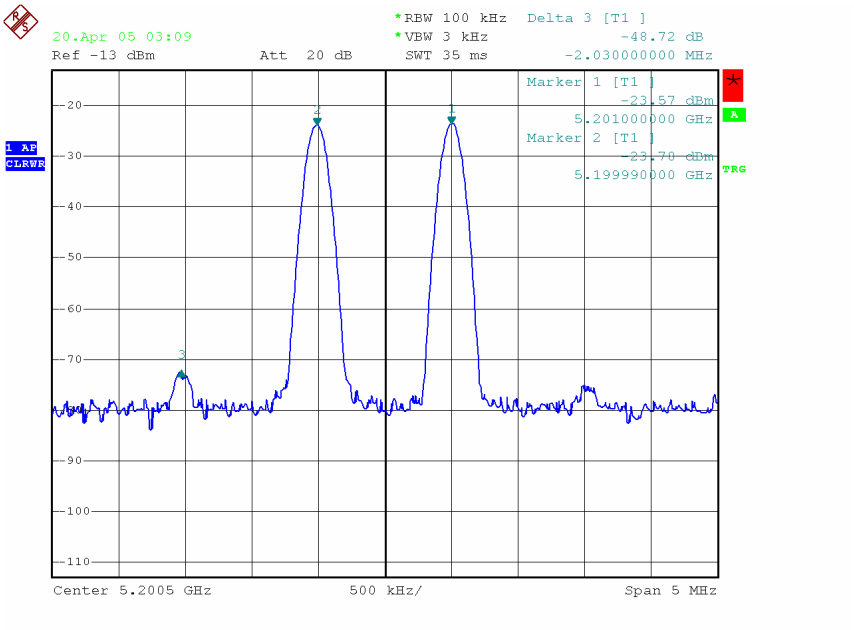
(a) S21 - HGM



(b) S21 - LGM



(c) S12 - Isolation



(d) IIP3 – Two tone test

Figure 24. Measurement results for GCAB

Two-tone test was carried to measure the third order input intermodulation point (IIP3) of the GCAB circuit. The two tones selected to be in the higher gain region were at 5.2GHz and 5.201GHz, with 1MHz spacing. Fig 24(d) shows the result of the two-tone test and the IIP3 is measured from the fundamental and third order component power levels using [22],

$$IIP3 = \frac{\Delta_{(P1,P3)}}{2} - P_{in} \tag{6.2}$$

Using (6.2), the IIP3 was calculated to be -3 dBm.

6.4 Discussion and conclusion

An LNA with dual-mode operation has been designed for use in a DCR and features a simple and novel gain control technique and is believed to be the first work to integrate the gain control circuitry and active balun to reduce silicon real estate and thus help provide a compact, low cost and low power solution for 5 GHz ISM band receivers. Good performance from the balun and the LNA make this an ideal way of implementing the RF front end with low noise and a balanced RF output.

Measurements for silicon characterization have been challenging due to various issues mentioned before. However, the approach of on-wafer probing has proved successful and was used to characterize the active balun performance. Measurements on the wafer, however, do not have any matching networks included at the input and the output and hence show a broadband nature of plots. With the inclusion of matching networks on evaluation boards, the matching can be improved at the desired frequency and gain improved further. Gain and phase mismatch measurements will need to be done on-wafer because of the presence of a surface-mount balun on the evaluation board, used to convert the differential output into a single ended one, for ease of testing.

Demand for higher data bandwidth and low voltage design due to scaled devices will drive future markets for both LNA and mixer in RF transceiver design. With emergence of new standards like Ultra Wide Band (UWB) and multiple input multiple output (MIMO) systems, the industry is targeting even higher data-rates. Integration, power consumption, and low voltage will become very critical in the very near future. Therefore innovation and investigation of both novel LNA and mixer topologies have become very necessary.

Current and future work in RF transceiver design will have two major thrusts (i) investigation of low voltage solution for wireless receiver sub-components, namely, down-conversion mixer with high IIP3 and IIP2 values, low noise amplifier (LNA) with high gain and wide dynamic range, and half-rate quadrature LC VCO; (ii) Investigation of wireless transmitter sub-components which includes up-conversion mixer with good linearity and P1dB, RF switch with high isolation and low insertion loss, and linear highly efficient power amplifier. These sub-circuits will be a basis for low voltage and high linear RFICs for numerous future communication applications.

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