HIGH IIP2 CMOS DOUBLY BALANCED QUADRATURE SUB-HARMONIC MIXER FOR 5 GHz DIRECT CONVERSION RECEIVER

By

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To the Faculty of Washington State University:

The members of the Committee appointed to examine the thesis of PARAG UPADHYAYA find it satisfactory and recommend that it be accepted.

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Chair

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CMOS DOUBLY BALANCED QUADRATURE SUB-HARMONIC MIXER FOR 5 GHz DIRECT CONVERSION RECEIVER

ABSTRACT

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This thesis presents a new low power and high IIP_2 0.25-μm CMOS doubly balanced sub-harmonic mixer for 5 GHz Industrial Scientific Medical (ISM) band direct conversion - zero IF receiver. Using a ***½X*** LO frequency generation scheme the sub-harmonic mixer overcomes LO self-mixing problem common in conventional direct conversion receivers (DCR). Measurement shows the sub-harmonic mixer is able to achieve voltage conversion gain of 8.2 dB, input compression P_{1dB} of –8 dBm, IIP_3 of –2.5 dBm and IIP_2 of 36 dBm while consuming only 1.35 mA of DC current. Measured results correlate well with simulated results where the mixer is able to achieve high IIP_2 of 55.3 dBm, IIP_3 of –6.5 dBm, P_{1dB} of –12 dBm and voltage conversion gain of 8 dB including 1% g_m mismatch, 0.5% load mismatch and 2º LO phase error. The mixer takes up less than $1mm^2$ of silicon real estate including test die pads.

This work also gives an overview of direct conversion RF transceiver architecture and its design challenges and potential solutions for addressing 1/f noise, DC offset, 3^{rd} order intermodulation products and more importantly 2^{nd} order intermodulation in the mixer. Two novel CMOS doubly balanced quadrature sub-harmonic mixer architectures, which have high

immunity to 2nd order intermodulation products and achieves high IIP2 needed for DCR applications, are presented. While sub-harmonic are generally associated with microwave frequency design in 10s and 100s of gigahertz, a novel topology shows its viability for 5 GHz ISM band applications, which includes IEEE 802.11a and Hiperlan2 wireless LAN standards in the US and Europe, respectively. The design emphasizes trifecta of low power, low voltage, and low cost sub-harmonic mixer design that can be applied to CMOS and SiGe technologies. The mixer theory and design methodology presented can be also be followed as a design guide for developing high performance mixer circuits for many applications including superheterodyne transceivers and are not just limited to homodyne transceivers.

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Dedication

This thesis is dedicated to my parents who

dared to dream big for their kids

LIST OF ABBREVIATIONS

BPF	Band Pass Filter
BW	Bandwidth
CDBQSHM	CMOS Doubly Balanced Quadrature Sub-Harmonic Mixer
CMOS	Complementary Metal Oxide Semiconductor
CMRR	Common Mode Rejection Ratio
CP	Charge Pump
DCR	Direct Conversion Receiver
DCT	Direct Conversion Transceiver
DSB	Double-Sideband
F	Noise Factor
F_T	Unity Gain Frequency
FET	Field Effect Transistor
g_m	FET Transconductance
IF	Intermediate Frequency
IIP_2	Second order Input Intercept Point
IIP_3	Third order Input Intercept Point
IMD_2	Second order Intermodulation Product
IMD_3	Third order Intermodulation Product
IP	Intercept Point
P_{1dB}	Input 1dB Compression Point
PD	Phase Detector
PFD	Phase Frequency Detector
PSRR	Power Supply Rejection Ratio
LNA	Low Noise Amplifier
LO	Local Oscillator
LPF	Low Pass Filter
MOS	Metal Oxide Semiconductor
NF	Noise Figure
OFDM	Orthogonal Frequency Division Multiplexing
OIP_2	Second order Output Intercept Point
OIP_3	Third order Output Intercept Point
OOK	On Off Shift Keying
PA	Power Amplifier
PLL	Phase Lock Loop
QAM	Quadrature Amplitude Modulation
RF	Radio Frequency
RX	Receive
SSB	Single-Sideband
TL	Transmission Line
TR	Transmit/Receive
TX	Transmit
U-NII	Unlicensed National Information Infrastructure
VCO	Voltage Controlled Oscillator

SELECTED LIST OF PUBLICATIONS

1. P. Upadhyaya, M. Rajashekharaiah, D. Heo, Y. E. Chen, "A New 5-GHz ISM Band CMOS Doubly Balanced Sub-Harmonic Mixer for Direct Conversion Receiver," *Proceeding, IEEE European Conference on Wireless Technology*, pp. 65-68, October 2004.

2. M. Rajashekharaiah, P. Upadhyaya, D.Heo, Y. E. Chen, "A 5GHz LNA with New Gain Controllable On-Chip Active Balun for ISM Band Applications," *Proceeding, International Conference on Solid-State and Integrated Circuits Technology*, vol. 2, pp. 1252-1255, October 2004.

3. P. Upadhyaya, M. Rajashekharaiah, D. Heo, Y. E. Chen, " "A New 0.25-µm CMOS Doubly Balanced Sub-Harmonic Mixer for 5-GHz ISM Band Direct Conversion Receiver," *Proceeding, International Conference on Solid-State and Integrated Circuits Technology,* vol. 2, pp. 1295-1298, October 2004.

4. M. Rajashekharaiah, P. Upadhyaya, D. Heo, "A compact 5.6 GHz low noise amplifier with new on-chip gain controllable active balun," *IEEE Workshop on Microelectronics and Electron Devices*, pp.131-132, April 2004.

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6. P. Upadhyaya, M. Rajashekharaiah, D. Heo, Y. E. Chen, " A High IIP2 Doubly Balanced Sub-Harmonic Mixer in 0.25-µm CMOS for 5-GHz ISM Band Direct Conversion Receiver," *IEEE RFIC Symposium*, June 2005.

7. M. Rajashekharaiah, P. Upadhyaya, D.Heo, Y. E. Chen, "A 5GHz New Gain Controllable On-Chip Active Balun for ISM Band Applications," *IEEE International Symposium on Circuits and Systems*, May 2005.

8. P. Upadhyaya, M. Rajashekharaiah, Y. Zhang, D. Heo, Y. E. Chen, "A 5 GHz Novel 0.18-um Inductor-less CMOS Sub-Harmonic Mixer," *IEEE Workshop on Microelectronics and Electron Devices*, pp. 71-74, April 2005.

9. P. Sun, L. Wang, P. Upadhyaya, D. Heo, "High Isolation 10 GHz to 20 GHz SPDT Switch Design using Novel Octagonal PIN Diode Structure," *IEEE Workshop on Microelectronics and Electron Devices*, pp. 38-41, April 2005.

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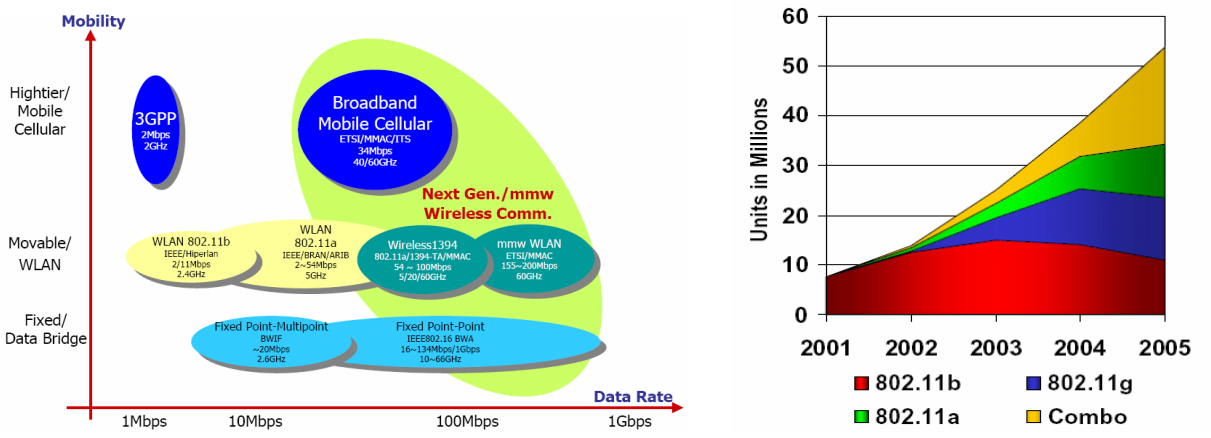
1.0. INTRODUCTION

Data communication, specifically, wireless and wired, more specifically, optical communications are the engines for the future. These market areas have grown exponentially in recent years and are expected to grow at similar rates into the very distant future. The insatiable desire for higher bandwidth and data rates have challenged the hardware industry, which forms the backbone of both wired and wireless communication, to develop faster and innovative low cost integrated chip solutions to help foster this growth. In the fast growing wireless industry 54 Mbps communication have already been achieved and are backed by IEEE 802.11a and Hiperlan2 industry standards utilizing the unlicensed 5 GHz ISM (Industrial Scientific and Medical) frequency bands (see Figure 1-1). The low cost integrated circuits solutions for these markets are therefore a significant engine for this growth, which demands constant innovations.



(a) **(b)**

Figure 1-1: (a) Data communication rates (b) Market growth in IEEE 802.11a/b/g transceivers

The bulk of this market growth is, for that reason, is primarily focused on a single chip low cost, low power, and highly integrated RF CMOS direct conversion transceiver (DCT). The DCT are highly integrated compared to widely used superheterodyne RF transceiver architectures

which also includes very low IF (intermediate frequency) transceivers. Furthermore, the DCTs are reconfigurable and can accommodate past (IEEE 802.11 b&g) and next generation wireless communication standards such as the emerging Multiple Input Multiple Output (MIMO) for achieving high data rates. The block diagram of a conventional DCT is shown in Figure 1-2.

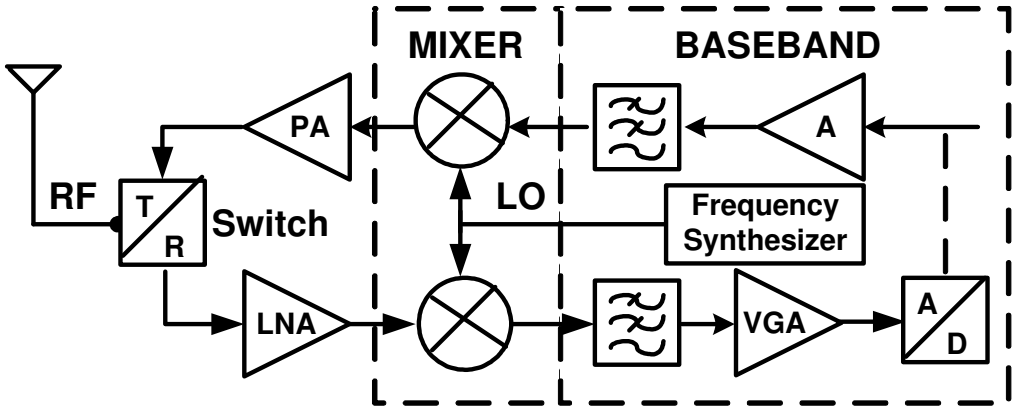


Figure 1-2. Direct conversion transceiver (DCT) block diagram

The design challenges, however, goes hand in hand with DCT advantages. Most direct conversion receivers (DCRs) in DCTs suffer degradation of signal to noise ratio (SNR) performance due to well known problems of local oscillator (LO) self-mixing which causes static and dynamic DC offset, 2nd and 3rd order intermodulation distortion, and low frequency flicker noise or the 1/*f* noise [1]-[4].

1.1. LO Self-Mixing

The LO self-mixing in DCRs is due to inadequate on-chip isolation which allows strong LO signals in the mixer to couple through the silicon substrate to the RF port of the mixer, the low noise amplifier (LNA), and the RF antenna to "self-mix" with itself at the mixer LO port to generate static and dynamic DC offset voltages near the desired baseband mixer output (IF port) [3]. The LO leakage to the LNA and the RF mixer ports through silicon substrate generally

introduces static DC offset at the IF baseband but the LO leakage radiated through the RF antenna reflected by near and far moving objects introduces time varying or dynamic DC offset (see Figure 1-3).

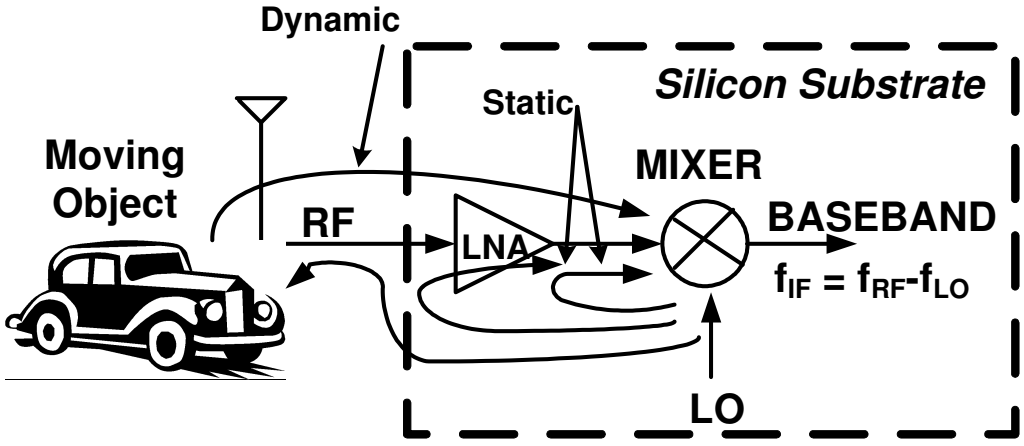


Figure 1-3: LO self-mixing mechanism in the DCR.

This dynamic offset complicates any attempted DC offset cancellation scheme at the output of the mixer since it is difficult to differential it from the time varying desired signal. This DC offset along with the mixer and the LNA non-linearity introduces many design challenges such as harmonic generation, gain compression, desensitization, blocking, intermodulation in DCR design. The 1/f or flicker noise, a low frequency noise, affects all CMOS RFICs and is another challenging problem in the DCR design. The intermodulation due to non-linear behavior of RFICs, discussed in later chapters, are classified into two different categories; odd and even. In DCRs both odd (IMD_3, IMD_5,…) and even intermodulation (IMD_2, IMD_4,...) are important. The causes of 2^{nd} order intermodulation (IMD_2), in particular a big concern in DCR, are numerous but include LO-RF leakage which cause LO self-mixing; strong interference due to adjacent channels; device mismatch parameters such as threshold mismatch, transconductance (g_m) mismatch, load mismatch; and any other asymmetry in the mixer circuit [3], [4] (see Figure 1-4).

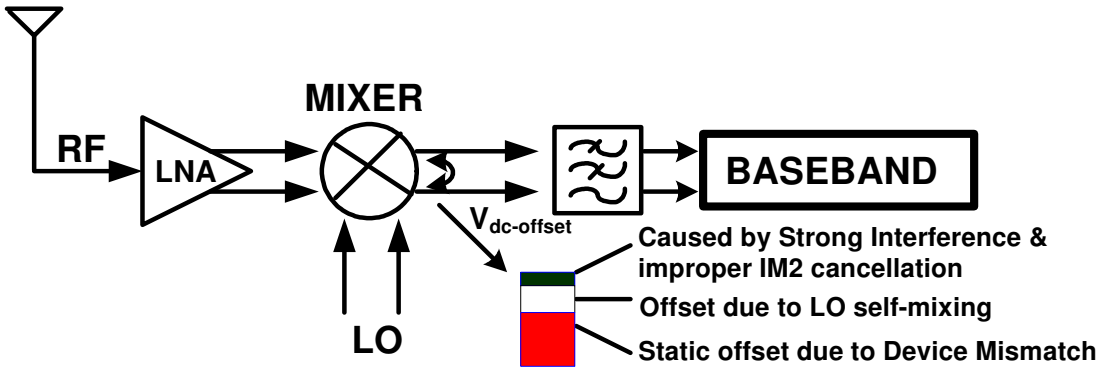


Figure 1-4. DC offset mechanisms in the DCR.

1.2. Thesis Objective

The primary focus of this work will be on the design of novel CMOS sub-harmonic mixer circuit architectures in the DCR to achieve high linearity, and therefore, low 2nd order (IMD_2) and 3rd order (IMD_3) intermodulation products. A fully balanced sub-harmonic mixer mitigates the LO self-mixing and IMD_2 related problems by separating the LO fundamental and the RF frequency band. Therefore, any LO-RF leakage and subsequent direct down-conversion, does not appear as a DC offset voltage (static or dynamic) at the IF baseband resulting in improved signal to noise ratio (SNR) of the DCR. This, however, requires an LO generation scheme that translates the LO fundamental to the RF frequency band needed for direct down-conversion. The CMOS 5-6 GHz mixers previously implemented use some form of elaborate fractional based LO generation scheme that requires few cascaded multipliers and regenerative dividers [5], [6]. These solutions, however, can have large power consumption and large silicon real estate requirements. A highly integrated *½X* LO generation scheme utilizing balanced quadrature LO fundamental phases is implemented to form the highly linear doubly balanced sub-harmonic mixer in the CMOS technology node to achieves similar or better performance in the proposed 5 GHz ISM Band while being low power and low cost.

1.3. Thesis Organization

The thesis is organized into 7 chapters. Chapter 2 will discuss the RF receiver architecture while Chapter 3 will discuss mixer theory including linearity, gain, and noise. Chapter 4 will cover mixer architecture and LO generation techniques and Chapter 5 will present my work on the sub-harmonic mixer to mitigate LO self-mixing and other challenges including techniques to reduce IMD_3 and IMD_2. The Chapter 6 will be comprised of future research topics and suggested improvements and possibilities for low voltage inductor-less mixer using bias-offset transconductance linearization methods and finally, final thoughts and conclusions are summarized in Chapter 7.

2.0. RF RECEIVER ARCHITECTURE

In last 20 years the communication industry has been radically transformed with improvements in communication technology, methods and theory. The transformation has been directed by consumer demand for low cost and higher data rate communication that offers just about everything. This is especially more so in the hand-held wireless devices, now a norm in the 21st century, where size, power, cost and functionality are targeted goals. 'The Supersonic Heterodyne Receiver' was invented by Edwin Armstrong in 1918 and is the most common architecture since its inception and is even pervelent now [7]. A typical superheterodyne receiver is shown in Figure 2-1.

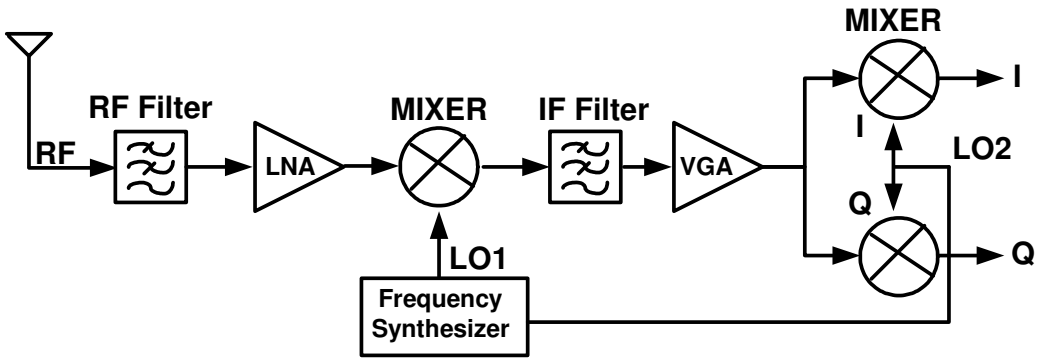


Figure 2-1. A typical superheterodyne receiver architecture.

In a superheterodyne receiver, the incoming RF signal is filtered and then amplified before frequency down-conversion by mixing the RF frequency with a LO (local oscillator) frequency. The frequency down-converted signal or the intermediate frequency (IF) is then filtered to remove the image signal and down converted again to baseband for demodulation and data recovery. While this architecture is simple and easy to design there are limitations on high integration due to the filter requirements to eliminate the image signal [8]. The high-Q IF filters and the RF image rejection filter are difficult to realize in silicon and therefore off-chip

components are required. Therefore the superheterodyne architecture which may also have multiple down-conversion stages are not highly integrated and are not a system-on-a-chip (SoC) solution.

Another alternative is to design a variation of the superheterodyne receiver, very low-IF receiver. The very low-IF receiver has higher integration than conventional superheterodyne architectures owing to the fact the RF is down converted to very low frequency IF with a single mixing stage. However, image rejection is still a problem and generally for high performance very-low-IF receiver off chip channel selection and image rejection filters are still required.

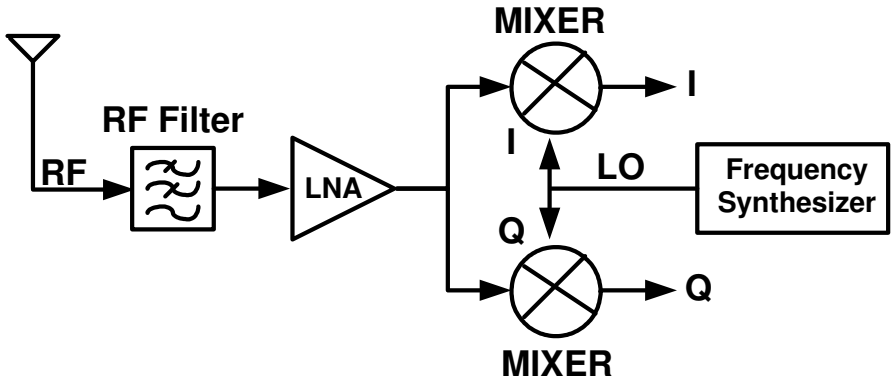


Figure 2-2. Direct conversion receiver (DCR) architecture.

A better and attractive solution is the direct conversion receiver or a homodyne receiver is shown in Figure 2-2. The advantages of this architecture are that it does not suffer from the image problem and does not need an image rejection filter and is architected to directly down-convert the RF signal to baseband or IF frequency is zero. This has potential for high integration and a single chip solution. Furthermore, the DCRs are multi-mode or reconfigurable and can accommodate past (IEEE 802.11 b&g) and next generation wireless communication standards such as the emerging Multiple Input Multiple Output (MIMO). This will be very important since the 21st century will be a century of integration for multi-mode, multi-functional and multi-

feature devices. Therefore added emphasis will be given to higher integration SoC multi-function and multi-feature solution in the future specially since cost of transistor scaling is increasing and much research is needed to overcome device and quantum limitations.

Many objections against direct conversion architecture have been stated mainly on the grounds of its dc-offset problem and even-order intermodulation rejection challenges. Since the signal is converted directly to baseband with the first mixing operation, DC offsets, flicker noise and second-order distortion from the mixer will all fall in the desired signal band. The DC offset, as explained in Chapter 1, includes contribution from the LO self-mixing due to inadequate on-chip isolation, circuit asymmetry, device mismatches and improper IMD_2 cancellation.

However, the static DC offsets can be handled successfully as presented using common mode feedback and load trimming methods in [9] and [10]. The dynamic DC offset due to LO self-mixing is resolved by choice of proper mixer architectures such as with sub-harmonic approach. A differential or balanced DCR topology can be employed to maintain circuit symmetry to reject common mode noise and for proper canceling of second order distortion (described in details in Chapter 3). Figure 2-3 shows the proposed balanced DCR approach.

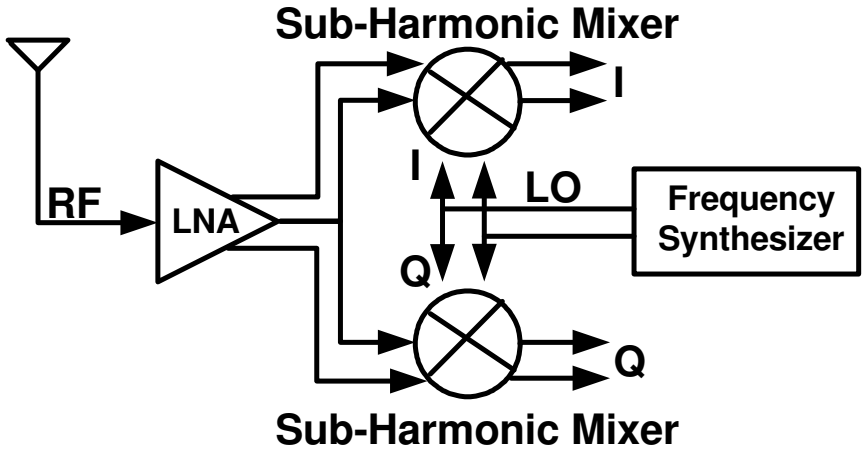
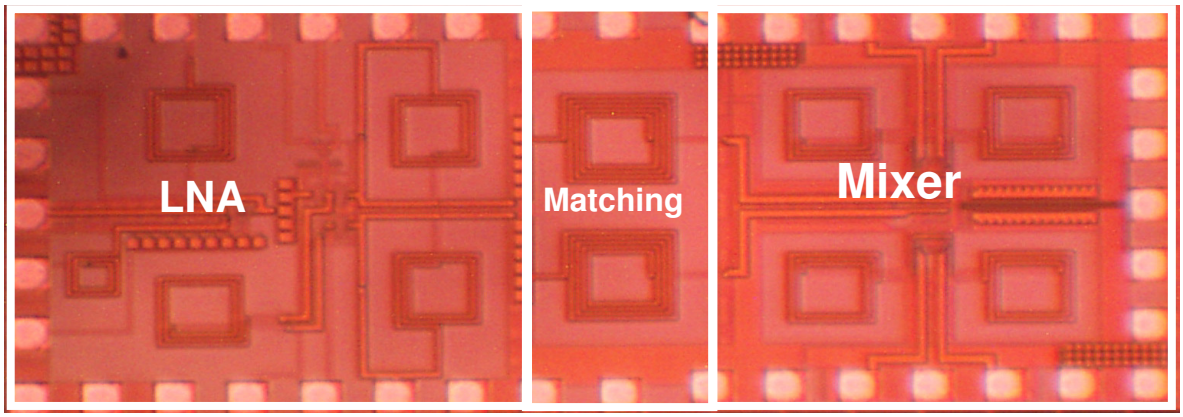
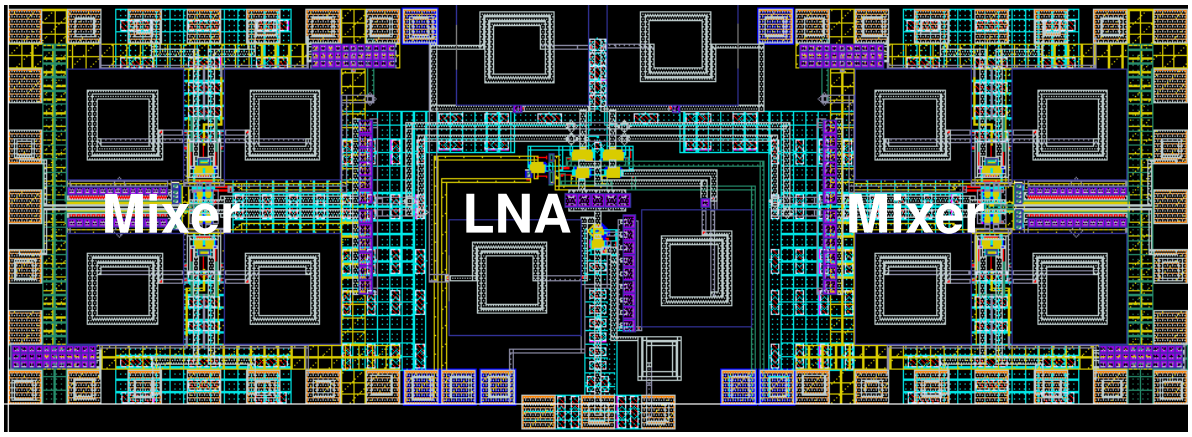


Figure 2-3. Balanced Direct conversion receiver (DCR) architecture.

A single input to differential output low noise amplifier (LNA), a differential mixer and a differential VCO (in the frequency synthesizer) is used to form the front-end of the balanced DCR as show in Figure 2-4. A schematic of a single-ended to differential output LNA is shown in Figure 2-5 and a differential and quadrature LCVCO are shown in Figure 2-6 and Figure 2-7, respectively. Proposed linear and balanced sub-harmonic mixer is discussed in Chapter 5 for use in DCR to help mitigate the challenges mentioned earlier. A micrograph of an I-Channel DCR front-end is shown in Figure 2-4 (a) and I/Q channel DCR layout is shown in Figure 2-4 (b).



(a)



(b)

Figure 2-4. (a) Micrograph of I-Channel DCR and (b) Layout of IQ-Channel DCR front-end

The quality of an RF receiver is measured primarily by its input dynamic range that measures its the input sensitivity and maximum allowable input power. A spurious-free dynamic range (SFDR) is commonly used and is defined as,

$$SFDR = \frac{2(IIP_3 - kT - NF - 10\log B)}{3} - SNR_{\min} \tag{2.0}$$

where, k is boltzman constant, T is the temperature, NF is the noise figure, B is the bandwidth, IIP_3 is the 3rd order input intercept point, and SNR_{min} is the minimum signal to noise ratio required for the receiver. As we will see the LNA generally determines the input sensitivity and mixer the maximum allowable input power in the RF receiver front-end.

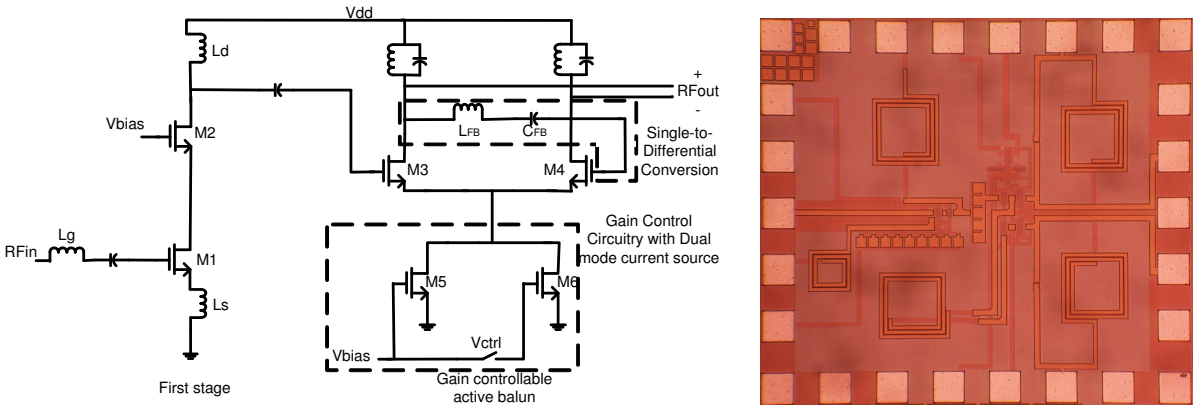
2.1. Low Noise Amplifier (LNA)

The front-end of the DCR must contribute very low noise to maintain high receiver sensitivity. The DRCs noise factor (F), a measure of noise, can be computed using Frii's relationship in Eq. (2.1) [8], [11]. Noise figure is noise factor in logarithmic form as in Eq. (2.2). Generally noise figure is used when describing noise characteristic of any RFICs.

$$F_{receiver} = F_{LNA} + \frac{(F_{MIXER} - 1)}{G_{LNA}} + \ldots + \frac{(F_N - 1)}{G_{LNA} * G_{MIXER} * \ldots * G_{N-1}} \tag{2.1}$$

$$NF = 10\log(F) \tag{2.2}$$

For maintaining high receiver sensitivity, the noise and gain of LNA (hence termed "low noise" amplifier) are very critical. High LNA gain is required to suppress noise contribution from the mixer and back-end components as shown by expression in Eq. (2.1). However, for modern wireless application the gain variability is also critical part of the LNA for achieving high input signal dynamic range or the range of acceptable RF signals input to the receiver. As in Eq. (2.0) lower input signal limit for the receiver is dictated by its noise figure and the upper limit by linearity of LNA and the mixer.



(a) **(b)**

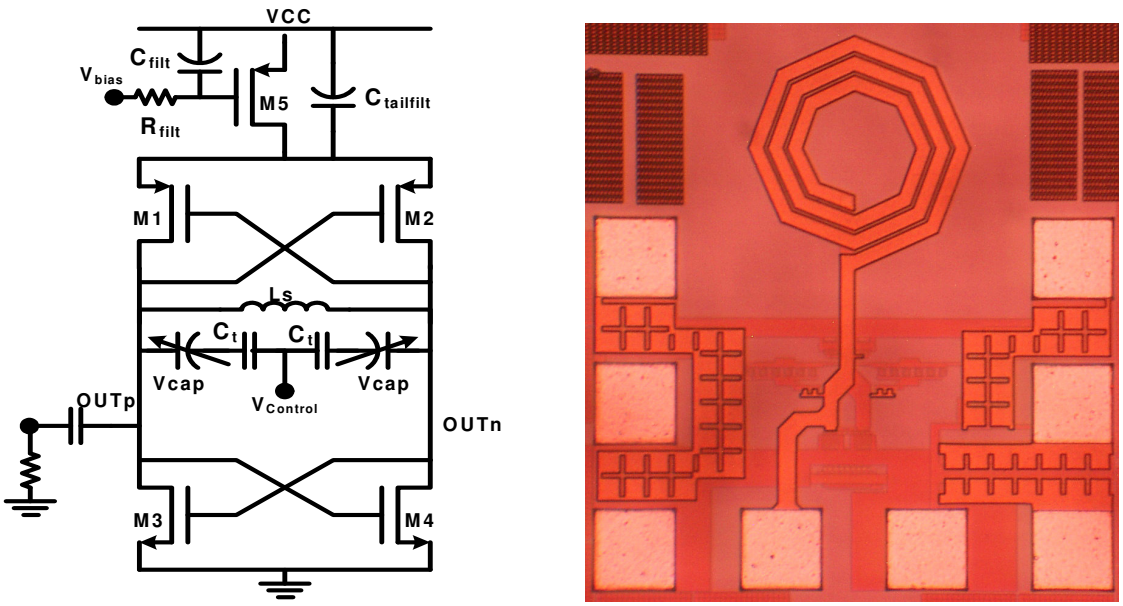
Figure 2-5. Dual gain LNA with active Balun for differential output: (a) circuit (b) micrograph of fabricated chip

The maximum acceptable input signal strength can be increased if the LNA gain can be reduced so not to saturate the mixer or not to exceed the mixer's linear range. Figure 2-5 shows a CMOS dual gain LNA fabricated in TSMC 0.25-µm technology with active Balun to achieve a desirable LNA, with high gain, low noise, dual gain modes; high and low, and a balanced output. [11].

2.2. Voltage Controlled Oscillator (VCO)

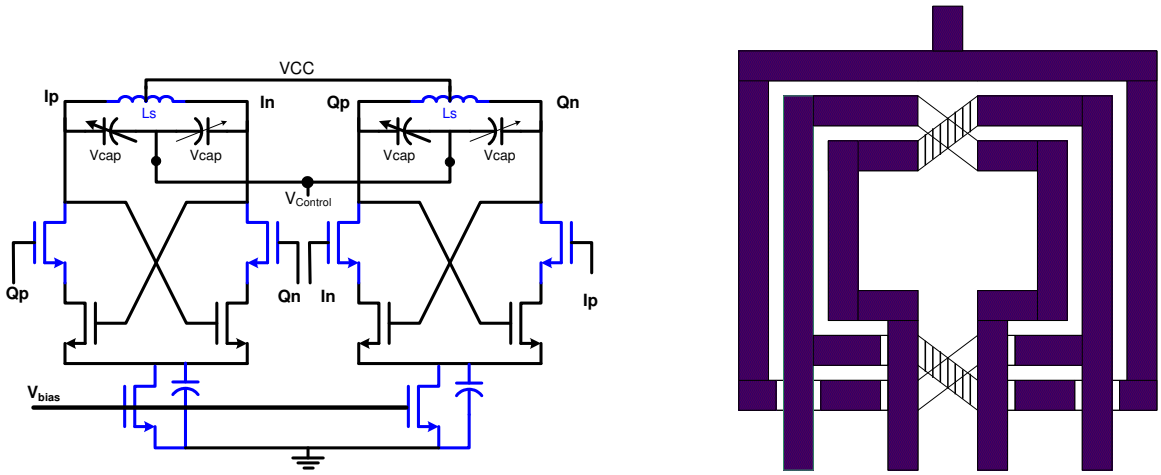
A voltage controlled oscillator is used to generate I/Q LO signal required in the DCR and also for the sub-harmonic mixer and is another critical component of the receiver since its limitation can adversely affect the DCR performance in terms of data bandwidth, harmonic distortion and spurious response. A direct conversion receiver with sub-harmonic mixing requires quadrature half-rate LO signals, as we will see in Chapter 5. One alternative is to use a single phase VCO as shown in Figure 2-5 and a poly-phase filter [8] to generate quadrature phases. However, phase mismatch, power loss, silicon area and added power consumption due to additional drive amplifier. Another approach is a VCO at RF signal frequency and a divide by 2

circuit to generate quadrature phases, however, for a single chip integrated solution the VCO and the PA (power amplifier) electromagnetic coupling will add to spurious noise in the transmitter and distortion in the receiver. The half-rate quadrature LC VCO is a better alternative to such a scheme.



(a) (b)

Figure 2-6. Complementary crossed-coupled VCO: (a) circuit (b) micrograph of fabricated chip



(a) (b)

Figure 2-7. (a) A Low voltage cascode quadrature LC VCO (b) 4-way center-tapped differentially coupled inductor in (a)

Te half-rate quadrature LC VCO is a better alternative to such a scheme. A quadrature VCO are low power and can have very good phase and amplitude accuracy as well as phase noise The IEEE 802.11a/b and Hiperlan2 standards using the Orthogonal Frequency Division Multiplexing (OFDM) based modulation scheme are more sensitive to phase noise than single carrier modulation scheme. The phase noise requirements come from two main considerations (a) interferer strength and (b) sensitivity of the OFDM scheme to phase impairments. For the highest data-rate of 54 Mbps, the standard uses 64-QAM with OFDM in a 20 MHz channel bandwidth which requires phase noise of at least –110 dBc/Hz at 1MHz offset [12].

A new low voltage cascode quadrature LC VCO (CQ) architecture shown in Figure 2-7 can be used. The CQ VCO has with lower *1/f* noise characteristic in addition to improved quadrature phase error performance without much degradation to phase noise. In CQ VCO the phase coupling transistor operating primarily in the linear region where *1/f* noise is low and additionally the CQ LC VCO utilizes a 4 way center-tapped differentially coupled inductor, as shown in Figure 2-7(b), for improved phase noise. In addition to low phase noise, the output power of the VCO has to be large since the LO signal is used to control a switch in the mixer. A large LO voltage signal is required to properly suppress second order effects in the mixer and to limit its flicker noise or *1/f* noise contribution by maintaining a large LO slew rate in the mixer.

3.0. MIXER THEORY

Mixer, as it names suggests, “mixes” or multiplies two signals to get a resultant output signal. A time domain multiplication is a convolution in frequency domain so, in the transceiver, mixers perform frequency translation or frequency up-conversion and down-conversion by multiplying an RF input signal, with frequency ω_{RF}, and an LO signal, with frequency ω_{LO}, present at mixers the RF and the LO ports, respectively. Ideally at the mixer IF output two distinct signal frequencies are present, one at $\omega_{RF} - \omega_{LO}$ and the other at $\omega_{RF} + \omega_{LO}$ as shown in Figure 3-1. The difference term is classified as the down-converted IF frequency and the summation term is considered the up-converted frequency. In transmitter, the mixer is used for up-conversion and in the receiver, the mixer is used for down-conversion. In a DCR, the mixer down-converts the RF signal from a particular radio carrier frequency directly to the baseband, such that, $\omega_{RF} - \omega_{LO} = 0$ Hz, in a single mixing stage.

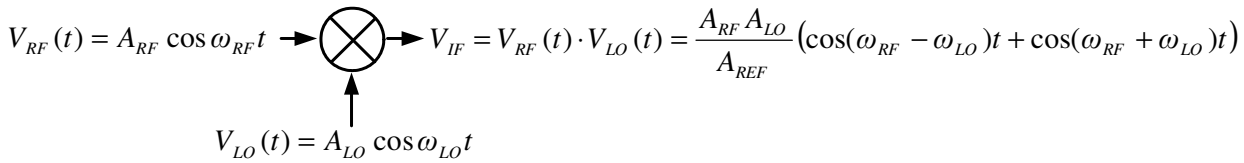


Figure 3-1. Ideal mixer response when single tone frequency inputs are applied.

As in Figure 3-1, the mixer, aside from performing frequency multiplication or translation, can provide amplification or attenuation. A passive mixer generally attenuates signal amplitude when translating RF signals to IF whereas an active mixer is generally used for signal amplification or to provide gain. The selection of mixers are application based and depends on other mixer performance parameters such as noise figure, linearity, and power consumption. Those are discussed in detailed later in this Chapter. In physical realization mixing and frequency multiplication are nonlinear operations by nature. Generally in DCR for maintaining

high input dynamic range the active mixer is used to supplies noise. Although the nonlinear characteristic is essential to mixers, their signal handling capacity is limited due to their nonlinearity at large signal amplitudes, which in turn generates undesirable odd and even harmonic distortion products and other fractional intermodulation distortion that can reduce the SNR of a receiver. Furthermore, in radio receivers, in which nearby channels are also occupied, the nonlinearity can lead to the aliasing of the power from the nearby channels to the receiver passband. The RF receivers and their building blocks require large input dynamic range and therefore mixer must be sufficiently linear. Generally passive mixers have good large signal handling capability while for active mixers achieving high linearity is always a challenge.

3.1. Mixer Linearity

Linear circuits are defined as those for which the superposition principle holds, i.e., if input $x_1(t)$ and $x_2(t)$ are applied separately to a circuit having responses $y_1(t)$ and $y_2(t)$, respectively, the response to the excitation $ax_1(t) + bx_2(t)$ is given by expression $ay_1(t) + by_2(t)$, where a and b are arbitrary constants [8]. By this definition as long as the system response is a linear combination of the input, the system is linear. However, all electronic circuits are nonlinear, some more weakly nonlinear in their actual ranges of operation than others. In analog and RF application the transfer characteristic of nonlinear and memoryless circuits can be described by a power series expansion in equation (3.0).

$$y(t) = \alpha_0 + \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + \ldots + \alpha_n x^n(t) = \sum_{m=0}^{n} \alpha_m x^m(t) \qquad (3.0)$$

Power series coefficient, α_0, corresponds to the DC term or offset while, $\alpha_{0\ldots}\alpha_n$, coefficients are the amplitudes associated with higher order terms. For weakly nonlinear circuits, the power series can be limited to include only up to third order nonlinear terms ($\alpha_{0,1,..3}$), however, for

strongly nonlinear circuits like power amplifiers, higher order terms are needed to accurately model the nonlinear behavior. If the input signal $x(t)=A\cos\omega t$, is applied to a weakly non-linear memory-less system with response in Eq. (3.0), with no DC offset to start out with, i.e. $\alpha_0=0$, then,

$$\begin{aligned} y(t) &= \alpha_1 A\cos\omega t + \alpha_2 A^2\cos^2\omega t + \alpha_3 A^3\cos^3\omega t \\ &= \alpha_1 A\cos\omega t + \frac{\alpha_2 A^2}{2}(1+\cos 2\omega t) + \frac{\alpha_3 A^3}{4}(3\cos\omega t + \cos 3\omega t) \\ &= \frac{\alpha_2 A^2}{2} + (\alpha_1 A + \frac{3\alpha_3 A^3}{4})\cos\omega t + \frac{\alpha_2 A^2}{2}\cos 2\omega t + \frac{\alpha_3 A^3}{4}\cos 3\omega t \end{aligned} \tag{3.1}$$

Table 3-1. Summary of power series expansion of weakly non-linear system

Frequency	Amplitude
DC	$\frac{\alpha_2 A^2}{2}$
ω	$\alpha_1 A + \frac{3\alpha_3 A^3}{4}$
2ω	$\frac{\alpha_2 A^2}{2}$
3ω	$\frac{\alpha_3 A^3}{4}$

The fundamental signal amplitude at the output is given by $(\alpha_1 A + 3\alpha_3 A^3/4)$ term and the even order harmonic and 3rd order harmonic are given by $\alpha_2 A^2/2$ and $\alpha_3 A^3/4$ terms, respectively. As seen from Table 3-1, the amplitude of the fundamental, even and 3rd order signals depend on power coefficients ($\alpha_{1,..}\alpha_3$), whose, determination is not very trivial and are dependent on biasing, technology parameters, and accurate continuous models. If non-linear elements are used in the system such as transistors, power coefficients depend on continuous device models which depends on inclusion of 2nd and 3rd order effects such as velocity saturation, mobility reduction, and other short channel effects.

If the excitation of a nonlinear system consists of several frequency tones instead of one tone demonstrated in Eq. (3.1), the modeling become more complex due to intermodulations resulting from interaction of multiple tones that results in linear combinations of all excitation frequencies and their harmonics. Generally for RF and analog systems a two-tone test is used to measure harmonic distortion resulting from intermodulation of the input terms. The output generally exhibits other harmonics components other than integer multiple of the input frequencies.

3.2. Two-Tone Test

A two-tone test is used to characterize the linearity behavior of the receiver RFICs including mixer and to determine signal blocking, desensitization. In the two-tone test, the input test signal consists of two sinusoids with frequencies closely spaced in the band of interest as shown in (3.2).

$$x(t) = A_1 \cos \omega_1 t + A_2 \cos \omega_2 t \tag{3.2}$$

When Eq (3.2) is applied to Eq. (3.0) for a weakly non-linear system it can be shown that,

$$y(t) = \alpha_1 (A_1 \cos \omega_1 t + A_2 \cos \omega_2 t) + \alpha_2 (A_1 \cos \omega_1 t + A_2 \cos \omega_2 t)^2 + \alpha_3 (A_1 \cos \omega_1 t + A_2 \cos \omega_2 t)^3 \tag{3.3}$$

When expanding the expression in Eq. (3.3) numerous spectral frequencies are produced and are commonly referred to as intermodulation products that have spectral content at frequencies,

$$\omega = m\omega_1 + n\omega_2; \quad |n| + |m| = order\ of\ intermodulation; \ n, m = \pm 1,2,3...k \tag{3.4}$$

Table 3-2 summarizes the amplitudes of the 2nd and 3rd order intermodulation products and Figure 3-2 shows the 3rd order intermodulation frequency spectra. The 2nd and 3rd intermodulation products appearing in the vicinity of the carrier frequency are critical in RFICs

for DCR since they are near the desired signal band and work to reduce the receivers SNR. The 2nd order products appear at frequencies $\omega_1 - \omega_2$ and $\omega_1 + \omega_2$ while the 3rd order products appear at $2\omega_1 \pm \omega_2$ and $2\omega_2 \pm \omega_1$.

Table 3-2: Summary of power series expansion of weakly non-linear system in response to two-tone test

Frequency	Amplitude
$\omega_1 \pm \omega_2$	$\alpha_2 A_1 A_2$
$2\omega_1 \pm \omega_2$	$3\alpha_3 A_1^2 A_2 / 4$
$2\omega_2 \pm \omega_1$	$3\alpha_3 A_2^2 A_1 / 4$

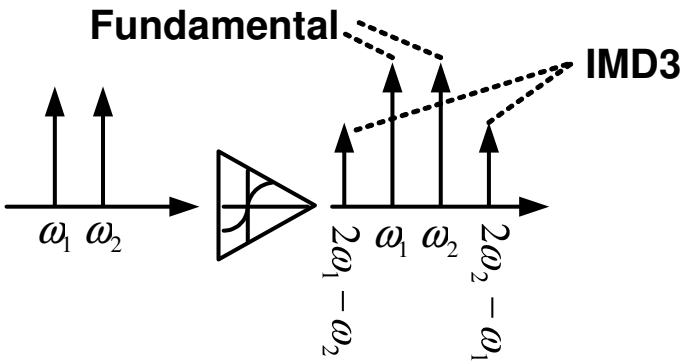


Figure 3-2. 3rd order intermodulation using two-tone test in a non-linear system

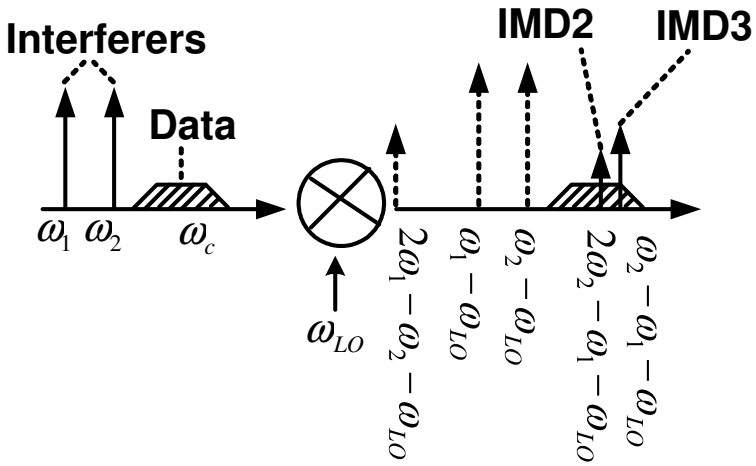


Figure 3-3. Noise products in desired band of DCR mixer due to intermodulation between interferers.

In mixer design, intermodulation distortion is key since physically this means that if a weak RF signal is accompanied by two strong interferers experiences 3rd order and 2nd order nonlinearity, the intermodulation products fall in the signal band to corrupt the desired signal as shown in Figure 3-3.

In RF circuits, therefore, intermodulation and the 1 dB compression point or P_{1dB} specifies the linearity. The measures of 2nd and 3rd order intermodulation are defined by the IIP_2, 2nd order input intercept point, and the IIP_3, 3rd order input intercept point, respectively. The IIP_2 is defined as the input power when the 2nd order intermodulation power is equal to the fundamental power while IIP_3 is an input power at which the 3rd order intermodulation product is equal to the fundamental as shown in Figure 3-4. The P_{1dB} specifies the input signal power at which the output single is compressed by 1 dB from ideal linear projection, i.e., the gain drops by 1 dB. At this compression point the system is considered weakly non-linear.

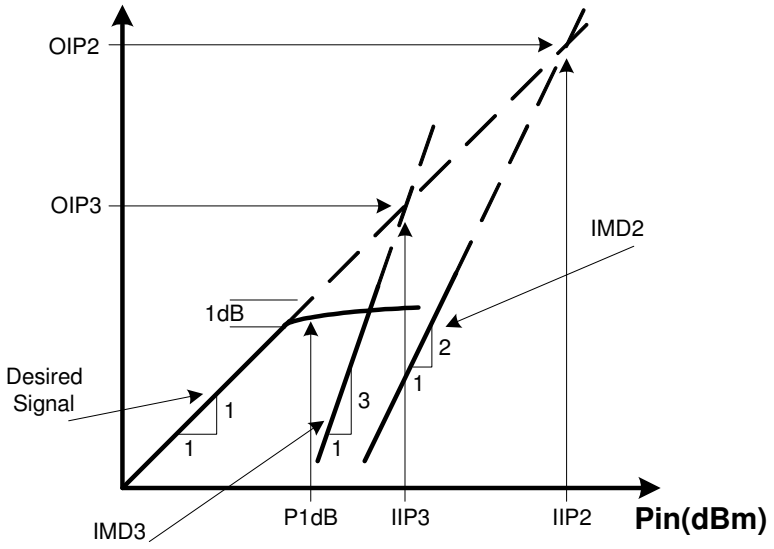


Figure 3-4. Graphical representation of IIP_2 and IIP_3 and P_{1dB}.

P_{1dB} can be computed from Eq. (3.1) as,

$$P_{1dB} = 10\log(0.145\left|\frac{\alpha_1}{\alpha_3}\right|) \tag{3.5}$$

The IIP_3 and IIP_2 can be also be expressed from Eq. (3.2) and Eq. (3.1) as,

$$IIP_3 = 10\log(\frac{3}{4}\left|\frac{\alpha_1}{\alpha_3}\right|) \tag{3.6}$$

$$IIP_2 = 20\log(\left|\frac{\alpha_1}{\alpha_2}\right|) \tag{3.7}$$

From Eqs (3.5) and (3.6) we can find relationship between P_{1dB} and IIP_3 which may be used to estimate one if another is known by

$$\frac{P_{1dB}}{IIP_2} = 10\log(\frac{0.145}{4/3}) \approx -9.64\,dB \tag{3.8}$$

So in general for weakly non-linear systems one can estimate that the IIP_3 will be about 9.64 dB lower than P_{1dB}. The input dynamic range or allowable RF signal range is determined by the mixer sensitivity that is limited by its noise in the lower-end and its linearity in the upper-end. Therefore, for a DCR it is important to have mixer with good dynamic range, especially in the upper-end, since large LNA gain can saturate the mixer or drive it beyond its linear range. The SFDR (spurious-free dynamic range) or the difference between $P_{RFin,min}$ and $P_{RFin,max}$ can be expressed as,

$$SFDR = \frac{2(IIP_3 - kT - NF - 10\log B)}{3} - SNR_{\min} \tag{3.9}$$

where, SNR_{min} is the required minimum signal to noise ratio. From Eq. (3.9) one can see high IIP_3 is desirable for the mixer along with low noise factor or figure to achieve high SFDR in the DCR. The receiver IIP_3 is given by Eq. (3.10), which shows that in the receiver the back-end components, mixers in DCR, dictate receivers IIP_3.

$$\frac{1}{IIP_3} = \frac{1}{IIP_{3,LNA}} + \frac{G_{LNA}}{IIP_{3,MIXER}} + \ldots + \frac{G_{LNA} * G_{MIXER} * \ldots * G_{N-1}}{IIP_{3,N}} \tag{3.10}$$

From Eq. (3.10) we can also stipulate that a variable gain LNA is preferred in the DCR to achieve maintain high receiver SFDR, i.e., a low gain is required to keep the RF signal power below the mixer's IIP_3 point and a high gain mode to improve input sensitivity by suppressing mixer noise. A low noise mixer can therefore aid in LNA design by allowing for lower LNA gain and hence a low power design. The plot in Figure 3-5 shows tradeoff between LNA gain and mixer noise figure and IIP_3 in a DCR front-end.

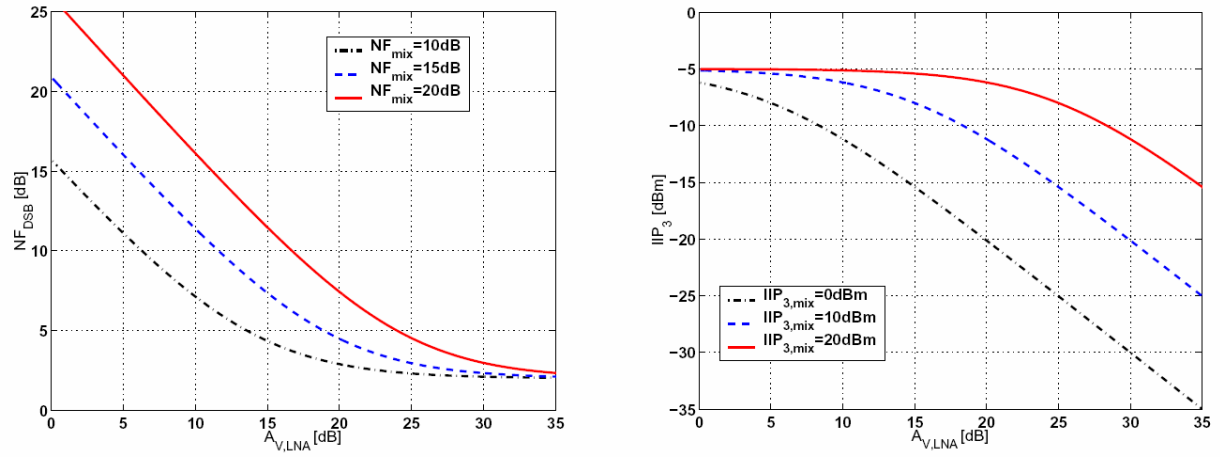


Figure 3-5. Plot showing mixers (a) noise figure (b) IIP_3 vs. LNA gain [12].

3.3. Mixer Noise

A low mixer noise can allow for lower power design especially in the LNA as mentioned in section 3.2 and shown by Figure 3-5. The noise of the mixer is generally measured by the noise factor and/or noise figure. The noise factor is the ratio of output SNR to input SNR, while, the noise figure is simply the noise factor in logarithmic scale. For direct down conversion receiver architectures the mixer noise is measured by double-sideband (DSB) noise figure as opposed to single-sideband (SSB) noise figure in image reject heterodyne receiver architectures.

In theory, the noise power of the down-converted signal is the same for both SSB and DSB but in the DSB case, the signal power is double when compared to single sideband in heterodyne, and therefore, the SNR and the noise figure is better for a DSB system compared to a SSB system by 3 dB.

Generally mixers have quite poor noise performance, usually the noise figures are over 10 dB. This is due to a combination of different noise sources that includes signal loss in the switching, noise contributed by harmonics and other distortion existing in the mixer output, supply noise, and device noise. The analysis of the mixer noise is not very trivial as in the case of LNAs, due to its time varying characteristics and other non-integer harmonic conversion products. However, in terms of mixer design for a DCR, one should focus on device noise, such as *1/f* or flicker noise, thermal noise, common mode noise and supply noises.

The flicker noise or *1/f* noise is a major concern in CMOS mixer design since flicker noise are low frequency noise (generally <1 MHz) and exist in the desired baseband IF frequency band. While the specific cause of flicker noise are not completely understood the general consensus is that it is caused by carrier generation and recombination due to surface traps in the silicon and silicon oxide interface. The flicker noise is therefore a function of surface area and is inversely proportional to FET geometry (*W, L*) and frequency (*f*) as shown in Eq. (3.11).

$$V_{n1/f}^2 = \frac{k_f g_m^{\ 2}}{WLC_{ox} f^{Af}} \tag{3.11}$$

Noise parameter, k_f, fitting noise parameter A_f, and device transconductance in Eq. (3.11) is generally included for comprehensive modeling of device flicker noise. The noise parameters k_f and A_f are voltage bias dependent terms and thus can be manipulated in mixer design for low flicker noise. To reduce flicker noise large active device geometry should be used, however, for high frequency RF application it is not always possible since device parasitic also scale up with

geometry, and thus, tradeoffs should be carefully considered. Another alternative to manage the effect of flicker noise is by selecting active mixer/circuit architecture as opposed to passive mixer solution to achieve large RF gain to suppress this noise. In a mixer large LO signals with high slew rates are also used to filter out some flicker noise but in general reducing 1/f noise is a difficult.

Another form of device noise is the thermal noise. Thermal noise is very well understood and is due to vibration of atoms and is modeled by a noise resistor, which is a function of temperature. All electric devices have thermal noise including resistors, transistors, capacitor and inductors since in physical realization they all resistive elements. The thermal noise contribution of resistors is given in Eq. (3.12), while transistor thermal noise is given in Eq. (3.13).

$$V_{n,resistor}^2 = 4kTR\Delta f \tag{3.12}$$

$$V_{n,transistor}^2 = \frac{8kT\Delta f}{3g_m} \tag{3.13}$$

From expression in Eq. (3.12) and Eq. (3.13) one can see that to reduce thermal noise in mixer circuit, smaller resistor values should be used and that transistor transconductance, g_m, should be maximized. The noise factor in Eq. (3.14) can be computed by considering the total device noise, which is the superposition of flicker and thermal noise, and thermal noise for other elements to calculate the total device noise figure of a mixer is given by Eq. (3.15).

$$F \approx 1 + \frac{V_{n,mixer}^{\ 2}}{4kTR_s\Delta f} \tag{3.14}$$

$$NF = 10\log(F) \tag{3.15}$$

The $V_{n,mixer}$ is the total noise of the mixer and R_s is the source resistance generally 50 Ω in RF systems. A hot-cold technique is commonly used to simulate and measure noise figure for the mixer [12].

4.0. MIXER ARCHITECTURE FOR DCRs

CMOS mixer architecture has long been investigated and generally the best suitable and most widely used architectures are based on a mixer first presented by Gilbert in 1968, now commonly referred to as the "Gilbert Mixer". The mixer presented by Gilbert was bipolar, as seen in Figure 4-1, however architecturally it can also be implemented in other technologies including CMOS. Within this context, the architecture discussion in this chapter is limited only to differential active topologies applicable for use in DCRs. The standard Gilbert mixer cell consists of two switching differential amplifiers composed of transistors Q3-Q4 and Q5-Q6 to form cross-coupled differential LO switching inputs, and a transconductance differential amplifier cell for RF inputs. The mixer load can be resistive or reactive and generally a current source is needed for a current-limited design.

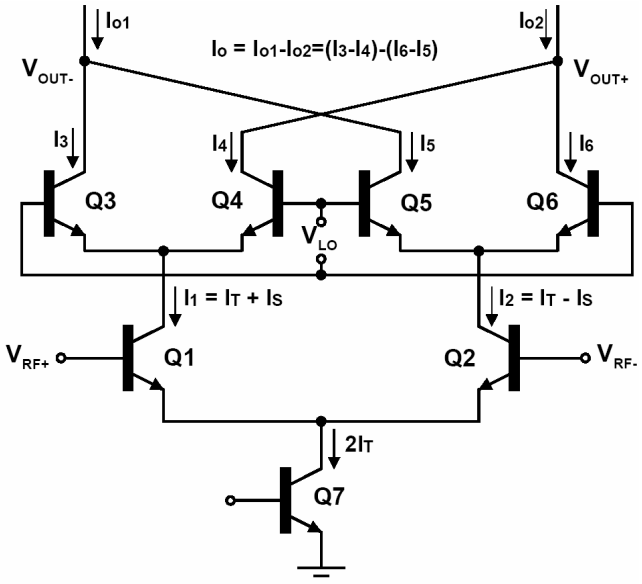


Figure 4-1. Bipolar Gilbert mixer [Gilbert, 1968]

The Gilbert mixer is considered double balanced since every aspect of the mixer circuit is differential which allows for very good common-mode noise rejection important in achieving low 2nd order distortion. The LO switching configuration allows for good isolation between the

LO port and IF output port, which is critical to minimizing LO-RF leakage, and also serves as isolating stage for achieving high RF-IF isolation. However, the LO-RF isolation is insufficient due to substrate leakage especially for high frequency application such as for 802.11a and Hiperlan2 coving 5 GHz ISM band. The LO self-mixing described in Chapter 1.1 allows for static and dynamic or time-varying DC offsets that are not easily removed with common-mode feedback DC cancellation circuitry. Therefore, a sub-harmonic mixer or fractional mixer architecture can be used to mitigate the LO-self mixing problem using a standard Gilbert mixer. With fractional or sub-harmonic mixing the LO fundamental frequency is different than the RF frequency and using a LO generation technique one can translate the LO fundamental to the required LO frequency equal to the RF frequency for direct down-conversion.

4.1 LO Generation Techniques for Sub-Harmonic Mixer

Translation to LO frequency from its fundamental tone required for direct conversion in the mixer can be achieved using techniques that include but are not limited to,

I. Even integer division

II. Fractional division

III. Multi-phase multiplication

IV. Proposed balanced multi-phase frequency doubler

These techniques can all be applied to mitigate LO leakage problem by having LO fundamental frequency at non-RF frequency and are discussed in detail in following sections.

4.2. Even Integer Division Technique

Even integer division LO generation techniques are based on having a VCO that operates at the RF frequency or two times the RF frequency and then dividing down by factor of two or four for IQ generation for sub-harmonic mixing.

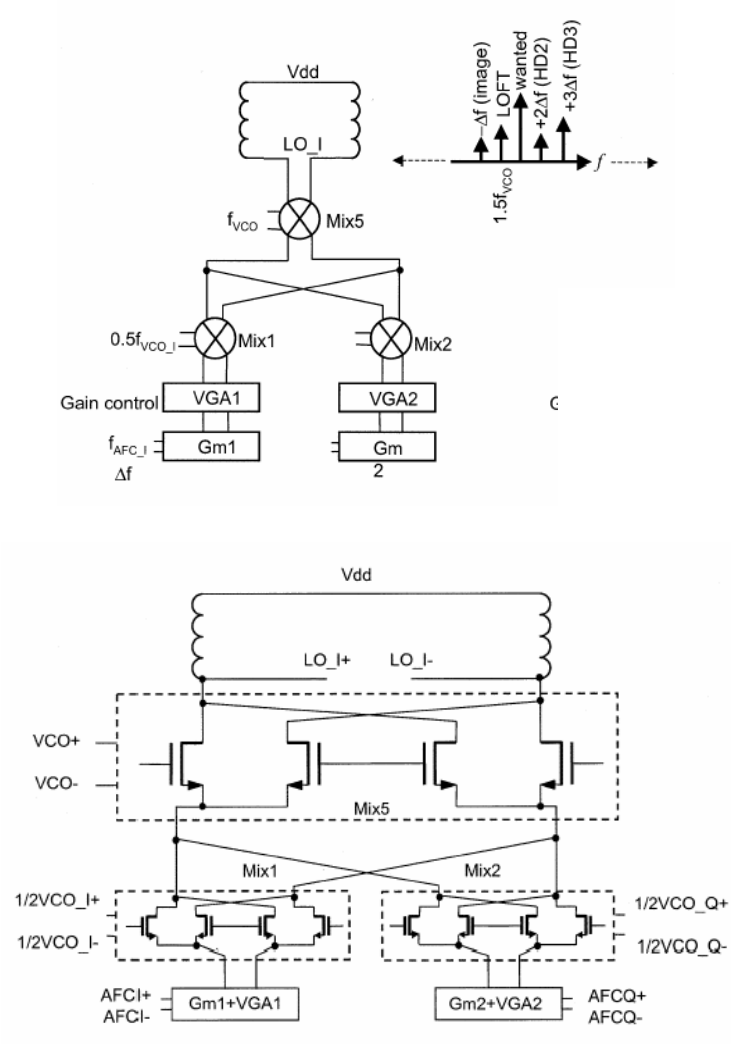


Figure 4-2. Even integer division techniques for LO generation implemented in direct conversion mixer [6].

While this solution is suitable for sub-harmonic mixing it generally requires larger silicon real estate and higher power consumption. The larger device count also means higher cumulative device noise and high noise figure. In Figure 4-2 implementation a VCO frequency is divided by two and mixed with itself to generate a LO frequency needed for direct down-conversion. Generally the high frequency dividers consume a lot of power to maintain high slew rates for the LO signals. Furthermore, for implementation shown in Figure 4-2, the voltage headroom requirements are relatively high due to the inherent architecture.

4.3. Fractional Division Technique

Fractional division techniques can be thought of as frequency planning method to reduce LO-RF leakage. Techniques generally involves use of a VCO that is outside the RF frequency band and dividers for division of VCO fundamental to generate the equivalent frequency needed for direct down-conversion which is the sum of the all the frequencies. Figure 4-3 shows the an example of fractional division method for proper LO generation where the VCO frequency (3.5 GHz) is mixed with a divided VCO frequency (1.75 GHz) to generate required LO signal frequency (5.25 GHz) for direct down conversion.

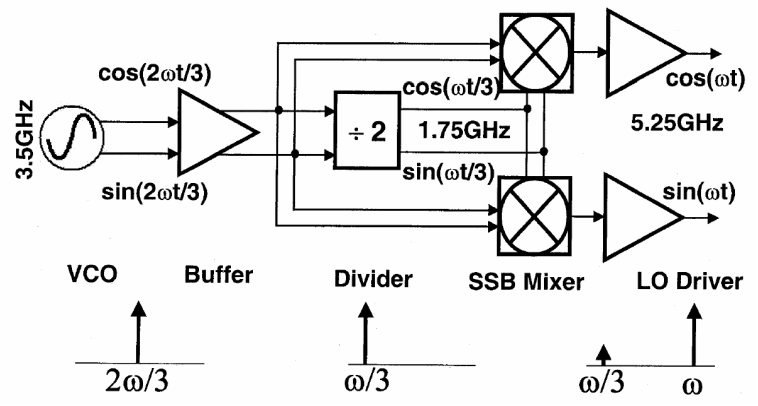


Figure4-3. Fractional division techniques for LO generation implemented in direct conversion mixer [5].

This techniques, however, has similar disadvantages as the even integer division method discussed in section 4.2. Additional mixing stages are required along with dividers for LO generation and as a result in the circuit implementation this technique requires high power and is a high real estate solution.

4.4. Multi-phase Multiplication Technique

The multi-phase multiplication techniques are good alternative and are widely considered for sub-harmonic mixers. The LO generation requires *N* number of $F_{LO,Fund}$ fundamental phases

at $180°/N$ to achieve a frequency of $f_{LO}=N*F_{LO,Fund}$. For a quadrature design $N=2$ is used. Generally N greater than two is not recommended since it demands larger silicon real-estate and puts more design complication on VCO design or poly-phase filter design. Figure 4-4 shows the method for LO generation in DCR application using quadrature LO fundamental phases.

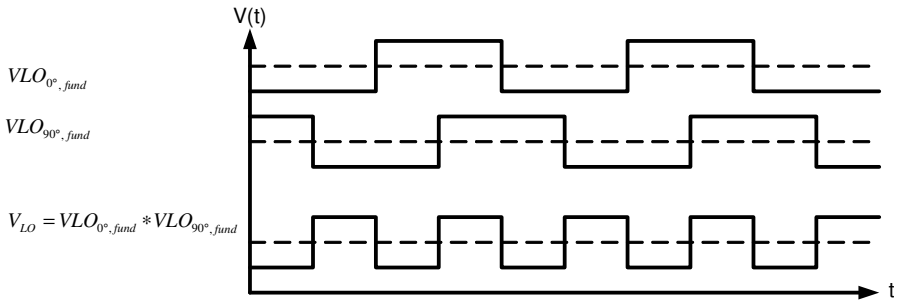


Figure 4-4. Quadrature multiplication for LO generation.

The LO is generated my multiplying two quadrature LO fundamental phases. In CMOS multiplication implementation can be achieved by two series FETs as in Figure 4-5. A singled balanced sub-harmonic mixer implementing this technique is shown in Figure 4- 5. A double balanced mixer using same circuit implementation requires another LO switching stage [13].

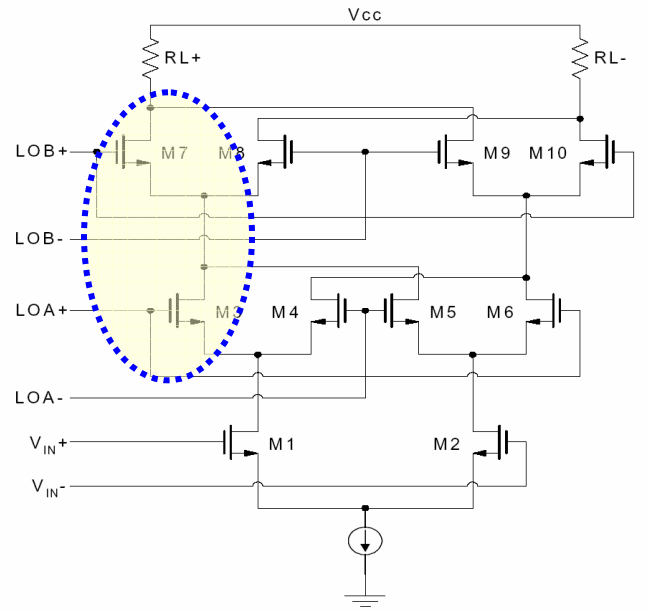


Figure 4-5. Simplified schematic of single-balanced sub-harmonic mixer using quadrature multiplication LO generation technique [13].

Another implementation using quadrature multiplication technique for LO generation in a doubly balanced sub-harmonic mixer is shown in Figure 4-6. Both sub-harmonic mixers in Figure 4.5 and Figure 4.6 are based on standard Gilbert mixer architecture integrated with a LO frequency generation circuit in the LO switching stage for direct down conversion. These topologies do well for DCR application, however, the silicon real estate usage is high owing to large transistor count and inductive degeneration (not shown in Figure 4-5 and Figure 4-6) for RF transconductance linearization. Also the noise figures of these mixers are also relatively high and these topologies are not suitable for low voltage application since there require four FET in series.

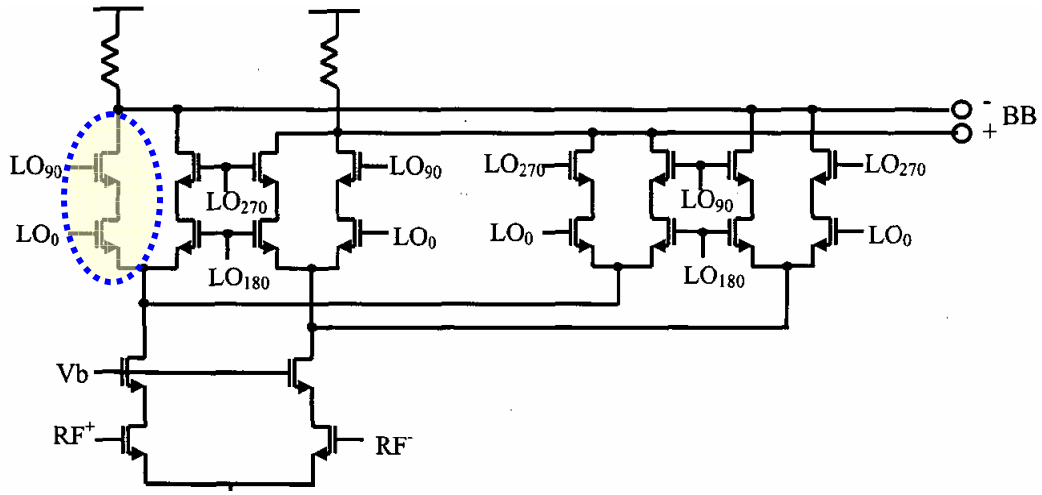


Figure 4-6. Simplified schematic of doubly balanced sub-harmonic mixer using quadrature multiplication LO generation technique [14].

4.5. Proposed Balanced Multi-phase Frequency Doubler Technique

A balanced multi-phase frequency doubler based on voltage to current conversion circuit is proposed for use in a sub-harmonic mixer. Figure 4-7 shows aforementioned simplified LO generation circuit topology using quadrature LO phases. The fully balanced signal for direct down-conversion is achieved through use of two fundamental LO differential quadrature phases

[L0n/p and L90n/p] and can be better understood by taking a closer look at the branch currents through transistors M1, M2, M3 and M4 in the mixer switching stage in Figure 4-8.

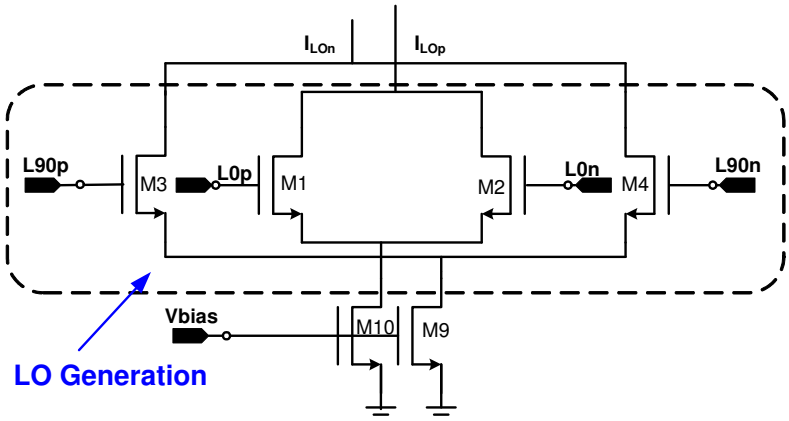


Figure 4-7. Simplified schematic of balanced quadrature frequency doubler circuit for LO generation.

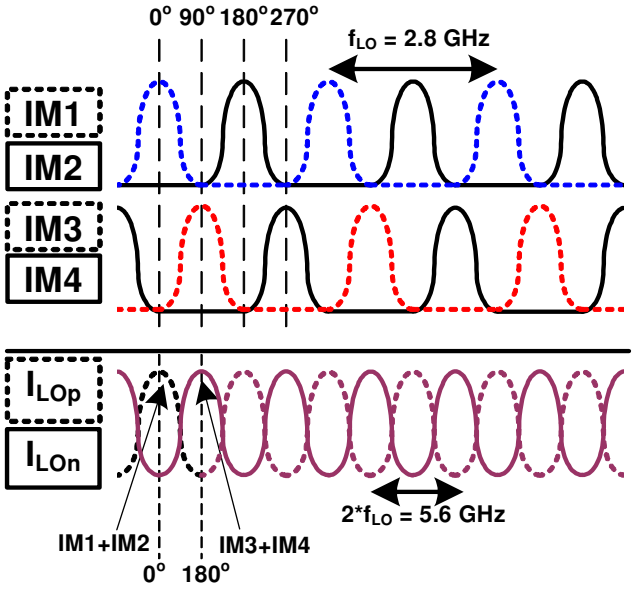


Figure 4-8. Branch currents IM1, IM2, IM3, IM4, I_{Lop} (sum of IM1 & IM2), and I_{Lon} (sum of IM3 & IM4) to demonstrate balanced frequency doubler technique.

Notice that the phase of current IM1, IM2, IM3 and IM4 are at 0°, 180°, 90° and 270°, respectively, corresponding to the applied quadrature LO fundamental voltage signals. The LO differential pairs act like good CMOS switches. When large differential LO signals are applied to

the gates, the branch currents switches (tilts) fully to one branch or to the other of the LO differential pair (see Figure 4-7). For example, when the LO differential signal L0p is high and complementary L0n is low, M1 FET is on and M2 FET is off, and the corresponding branch currents through M1 FET (IM1) is maximum, while IM2, the current through M2 FET, is near zero and vice-versa. The current I_{LOp}, the sum of IM1 and IM2 current, is then switching at twice (2X) the LO fundamental frequency. Similarly, the current I_{LOn}, the sum of IM3 and IM4, is also switching at twice the LO fundamental frequency. Since the differentially applied LO signals, L0p/n, are 90^o out of phase with L90p/n, the current I_{LOp} and I_{LOn} are 180^o out of phase with respect to one another. With the currents I_{LOp} and I_{LOn} going through the RF Gilbert mixing stage 180^o out of phase switching at twice the LO fundamental frequency, the double balanced sub-harmonic mixing is achieved at the mixer (IF) output.

This approach has several advantages over previously mentioned CMOS sub-harmonic mixers. The proposed ½ X LO generation using quadrature LO fundamental voltage to current conversion or frequency doubler technique avoids the elaborate fractional based LO generation scheme using multiple mixers and regenerative dividers as mentioned in Chapter 4.3 and Chapter 4.4 and therefore has low power and silicon real estate requirements. Furthermore, proposed LO generation technique offers advantages in terms of power, voltage headroom, noise, and transistor count. By reducing many transistors from the signal path, the mixer is expected to achieve better noise performance than the previously presented sub-harmonic mixers [5]-[6].

The sub-harmonic mixer pertaining to this thesis work is described in Chapter 5 and is an improvement over aforementioned sub-harmonic mixer architecture in all relevant performance parameters, which includes linearity, noise, and gain.

5.0. PROPOSED SUB-HARMONIC MIXER

Figure 5-1 shows the proposed CMOS doubly balanced quadrature sub-harmonic mixer (hereinafter, "CDBQSHM").

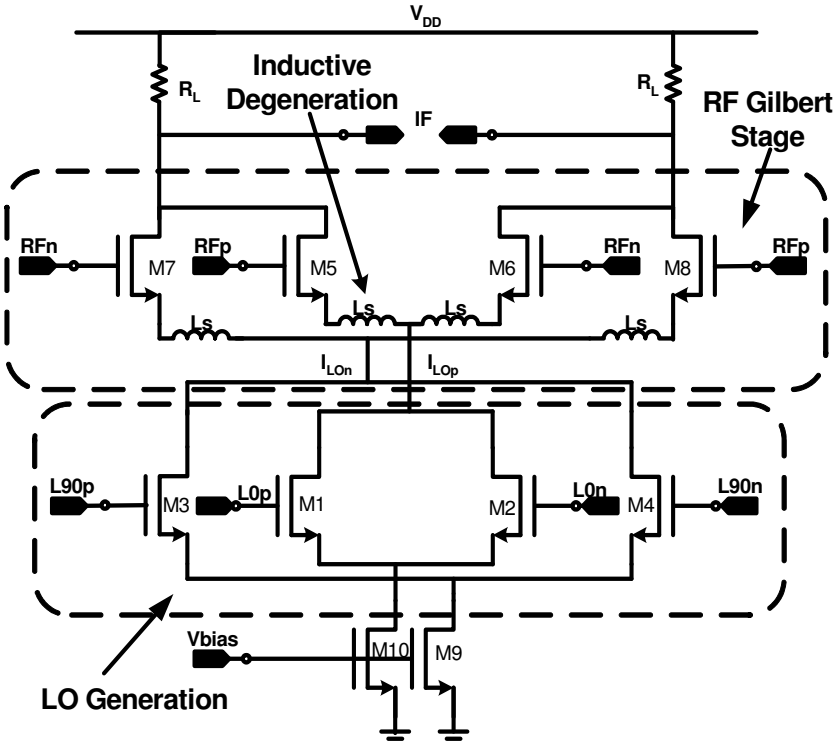


Figure 5-1. Simplified schematic of the proposed 5.6 GHz sub-harmonic mixer.

The CDBQSHM uses two differential fundamental square wave signals [L0n/p and L90n/p] at ½ RF frequency with 90º phase difference (quadrature phases) to generate the LO frequency at the RF frequency needed for direct down conversion. A voltage to current conversion frequency doubler circuit using quadrature LO fundamental phases is used for the sub-harmonic mixing as described in Chapter 4.5. While sub-harmonic mixer solutions for DCRs can be achieved with more than two differential phases (N=2,4,6..) separated by 180º/N phase difference, it is not recommended for applications in the 5-6 GHz frequency range. For N (number of differential LO phases needed for LO generation) greater than 2, the mixer circuit design becomes more complicated while requiring larger multiphase voltage controlled oscillator (VCO)

or larger polyphase filter. This can adversely affect the DCR performance in terms of noise and circuit mismatches, while increasing power consumption and silicon real estate.

The sub-harmonic mixing of the RF input with the LO inputs signal generated using our proposed frequency doubler technique discussed in Chapter 4.5 can easily be understood theoretically. Figure 5-2 shows the symbolic multiplication or mixing resulting from proposed sub-harmonic mixer using square devices, MOSFETs in saturation region, without consideration for common mode DC biasing. In the saturation region, for the MOSFETs, the current is proportional to square of the gate-source voltage as shown in Eq. (5.1). In the Figure 5-2, when a balanced (or differential) RF signal is applied to the gate and a balanced LO is applied in the source of MOSFETs, as it is for CDBQSHM, at the IF output we get multiplication of RF and LO as desired.

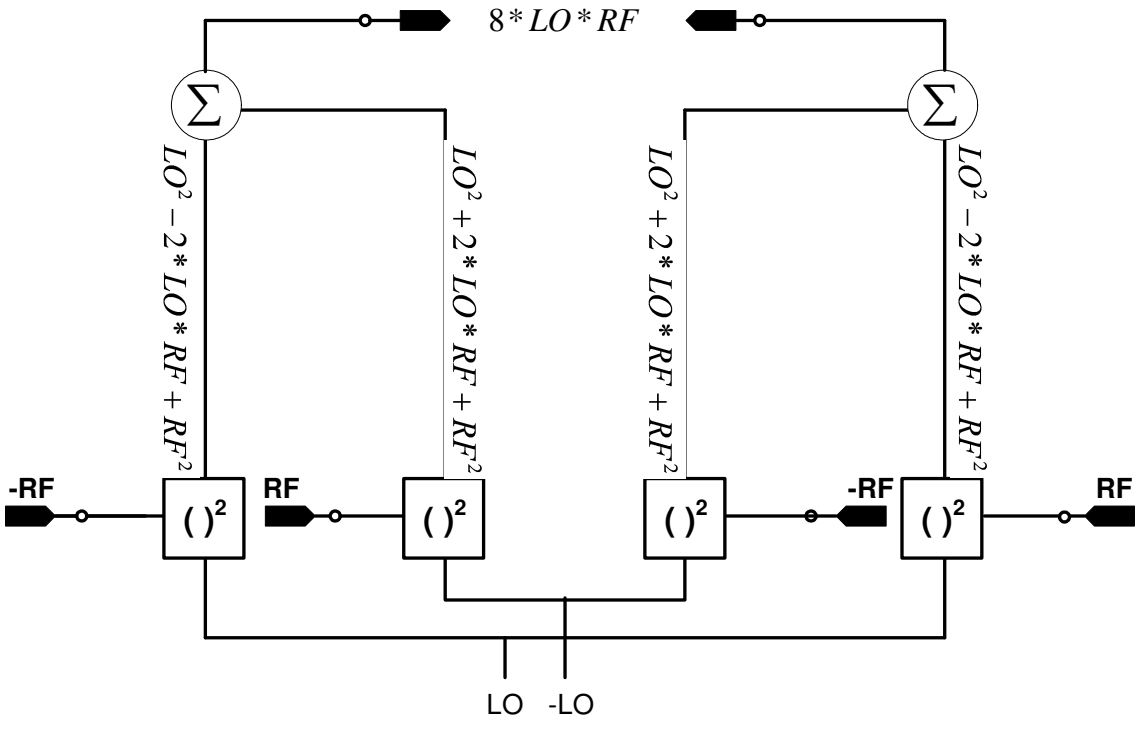


Figure 5-2. Symbolic mixing of sub-harmonic topology using square devices like MOSFETs in the saturation region.

Even with the inclusion of common mode DC voltages with the RF and LO signals, the mathematical expression for mixing is consistent with Figure 5-2 representation as shown in Eq. (5.0).

$$\begin{aligned}&\{[(CM_{LO}+LO)+(CM_{RF}+RF)]^2+[(CM_{LO}-LO)+(CM_{RF}-RF)]^2\\&-[(CM_{LO}-LO)+(CM_{RF}-RF)]^2+[(CM_{LO}+LO)+(CM_{RF}+RF)]^2\}\\&=8*LO*RF\end{aligned} \tag{5.0}$$

The Eq. (5.0) demonstrates that for given a LO signal at the source of the Gilbert RF stage, a proper mixing occurs between the LO and RF ports and at the IF output of the mixer only the desired baseband signal product are present and the common mode signals are rejected. The residual term ($2*V_{gs}*V_t$, V_t^2) in Eq. (5.1) due to multiplication between DC voltages (threshold and common mode voltages) and high frequency signals like RF and LO are eliminated when they are summed at IF port in the proposed doubly balanced circuit architecture. The square relations that result in undesired residual terms are due to MOSFETs I-V relationship in the saturation region where,

$$ID=\frac{KC_{ox}W}{2L}(V_{gs}-V_t)^2=\frac{KC_{ox}W}{2L}({V_{gs}}^2-2V_{gs}V_t-V_t^2) \tag{5.1}$$

The proposed CDBQSHM architecture using a voltage to current frequency doubler LO generation technique overcomes the numerous pitfalls of the conventional Gilbert based mixer (shown in Figure 4-1) including LO-RF leakage, which causes LO self-mixing. Overcoming LO self-mixing is critical in achieving robust IIP2 in DCRs. The CDBQSHM architecture is different than most Gilbert cell based sub-harmonic mixers [5]-[6] in that RF transconductance stage is in anti-parallel configuration with respect to the IF ports while the LO differential pairs (switching stage) are isolated from the IF port by RF differential pairs. The anti-parallel nature of the RF transconductance stage allows for very good RF-IF and RF-LO isolations and also RF stage

serves as buffer by isolating the IF ports from the LO ports to improve the LO-IF isolation. The CBDQSHM is fully balanced and has high common mode rejection ratio (CMRR) even in the 5 GHz ranges for which the mixer was design and this is very critical in achieving high IIP_2 performance.

5.1. Current Source Design and CMRR Considerations

The design of current sources is the prevailing factor for achieving high CMRR. The CMRR is defined as

$$CMRR = 20\log\left|\frac{Ad}{Ac}\right| \tag{5.2}$$

where, *Ad* is the differential gain and *Ac* is the common mode gain of the differential circuit. The common mode gain, *Ac*, of differential amplifier is inversely proportional to output conductance, g_{ds}, of the current source. Generally due to parasitic capacitance of the current source FET the

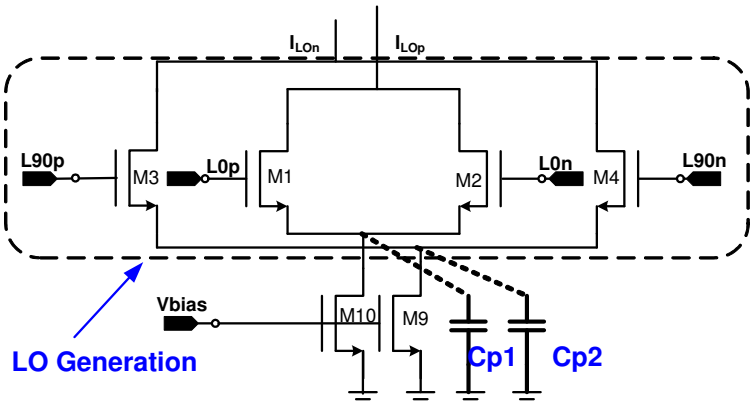


Figure 5-3. Parasitic capacitance at drain of current source works to reduces CMRR at high frequencies

output conductance increases with increasing frequency and as a result for higher frequency applications the CMRR is not as good as for low frequency applications. A low output conductance is maintained in CDBQSHM by designing multi-fingered current sources with large

gate length. Since output conductance is proportional to channel lengths modulation by using large device gate length the channel length modulation coefficient, λ, is reduced and low conduction is achieved as shown in Eq. (5.3).

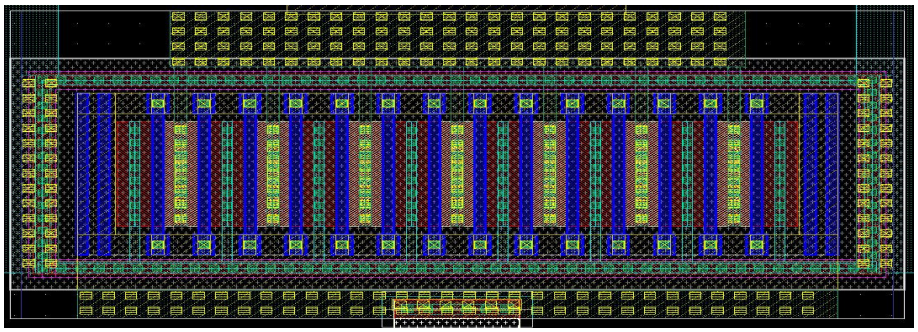


Figure 5-4. Multi-fingered NMOS current source layout to reduce drain parasitic

The multi-fingered current sourced is used to reduce the drain parasitic capacitance of the current source and hence improving high frequency CMRR performance. Figure 5-3 shows the layout of multi-fingered NMOS current source.

$$g_{ds} \approx \lambda I_D \tag{5.3}$$

Another consideration for achieving high CMRR is the differential gain. For low power design, achieving large gain in current limited region is important. However, there are trade-offs involving linearity that generally limits the differential gain in mixers, as we will soon see in Chapter 5.2. Another important factor in current source design is the flicker noise. As discussed in Chapter 3.3, the flicker noise is of great concern in DCRs and therefore the mixer must minimize the *1/f* noise contribution. Generally current sources are large contributors of flicker noise. To achieve low flicker noise the current source FETs have large geometries (*W* and *L*) and are biased at an optimum DC bias point where flicker noise is minimized. There is a limitation to how large you can make the current sources. Larger current source results in larger the drain parasitic and this can adversely affect the CMRR and IIP_2.

5.2. Mixer Gain and Linearity Considerations

There are numerous techniques that can be used to improve mixer linearity, some of which include pseudo multi-tanh transconductance linearization, bias offset linearization, passive and active negative feedback linearization to mention a few [15]. The best suited and also most widely used linearization techniques in CMOS mixers are the series feedback techniques, also commonly known as source degeneration method. In CDBQSHM series feedback or source degeneration inductor are used in the RF transconductance stage to improve linearity. The degeneration inductors adds very little thermal noise and has no significant cost to supply headroom, and therefore is a good choice. Additionally, the degeneration inductor helps in the RF port matching to standard 50Ω impedance by essentially providing additional phase lag between the applied gate voltage and the device currents and thereby turning the "impedance phasor" towards more real values. Adding degeneration marginalizes the dependence of gain on transistor transconductance of the RF amplifying stage and alternatively makes the gain a function of load and degeneration impedance as in Eq. (5.4). The magnitude of the effective differential transconductance can be modeled as common source amplifier with source degeneration, as shown in Figure 5-4.

$$G_m = \frac{g_m R_L}{1 + gmZ_{Ls}} \approx \frac{R_L}{Z_{Ls}} \tag{5.4}$$

The adverse effect of series feedback linearization used in CDBQSHM is that the gain is reduced. The first order small signal voltage conversion gain of the mixer can be modeling as,

$$A_v = \left| \frac{g_m R_L A_{LO} A_{RF}}{2 * (1 + gmZ_{Ls})} \right| \tag{5.5}$$

where, A_{LO} and A_{RF} are the amplitudes of the LO and the RF input signals, respectively. If the LO signal is driven as a large square wave signal then the conversion gain equation will can be

changed slightly by factor of a 2/π. The Eq. (5.4) and (5.5) expressions does not account for substrate consideration, which are also necessary for accurate conversion gain modeling.

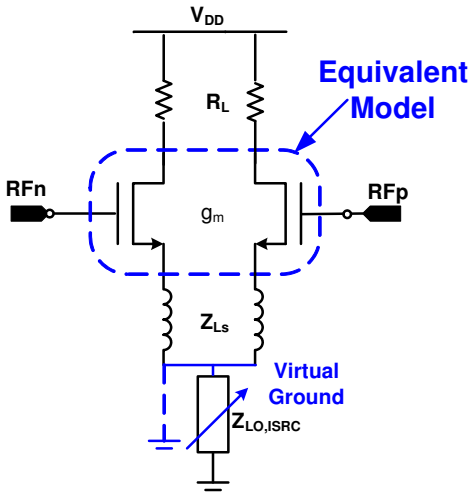


Figure 5-5. Equivalent model for the CDBQSHM for gain calculation.

Two different variations of the CDBQSHM mixer were initially created, a high linearity - low gain [HLLG] version and a medium linearity-high gain [MLHG] version. The HLLG is preferred for a DCR due to its linearity and adequate gain performance, and thus, is the primary focus of this thesis. This is because linearity translates to better IIP_3 and therefore better IIP_2 response in the DCR. Furthermore, Eq. (5.6) shows that the second order distortion voltage (V_{IIP2}) arising from third order intermodulation voltage (V_{IIP3}) terms between an input tone and "dc tone" due to offset voltage (V_{os}) can be lowered by increasing IIP_3 [16].

$$V_{IIP2} = \frac{V_{IIP3}^2}{4V_{os}} + V_{os} \tag{5.6}$$

Since the mixer architecture is sub-harmonic and is fully balanced high IIP_2 performance can be achieved in addition to aforementioned linearity improvements using series feedback technique. However, one should be cautious when to use source degeneration since it can have adverse effect on IIP_2 performance. From Eq. (5.2) we can see reduced differential gain also reduces the CMRR for the mixer.

Two variations of MLHG were designed with different degeneration inductors, rectangular and octagonal. An octagonal high quality factor (Q) inductor was designed using the ASITIC EM simulator and used to improve gain transfer and input matching performance over the rectangular inductors (~6), which was able to achieve return loss of 25 dB.

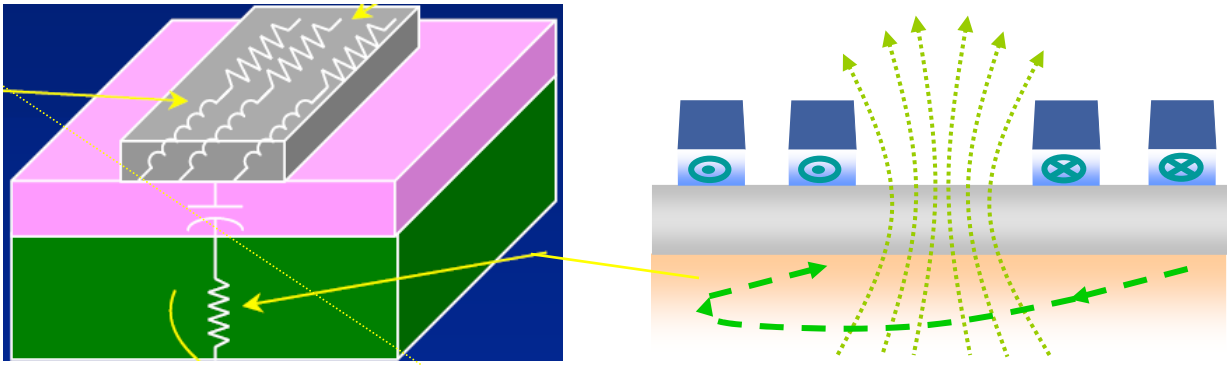
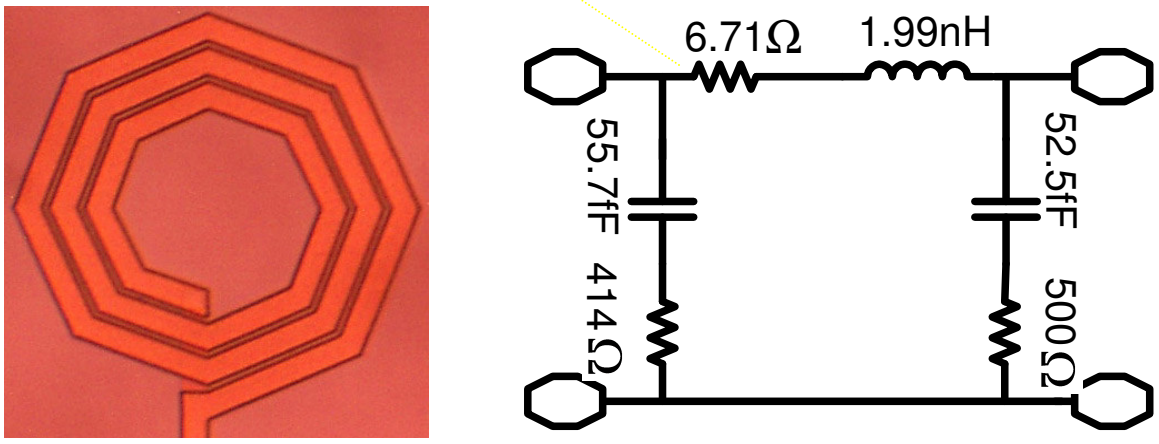


Figure 5-6. Eddy current substrate losses and parasitic losses in inductors [17]



(a) **(b)**

Figure 5-7. (a) Octagonal inductor layout (b) Lumped RLC model for inductor in (a) @ 5.6GHz

The quality factor of the inductor is limited by physical phenomena that converts the electromagnetic energy into heat and radiation and is a function of size and material. If the substrate is sufficiently conductive the bulk eddy currents flow (see Figure 5-5) in the substrate and present itself as a dominant form of loss and therefore, limits the Q [17]-[19]. Scaling the

inductor features such as the spirals inner diameter, conductor width, spacing between conductors and outer diameter can lower these substrate losses. To achieve high Q, optimization process should include keeping the inner diameter of the spiral large, using a higher number of turns, larger conductor width while maintaining relatively small outer diameter. Also the spacing between conductors should be carefully selected to reduce parasitic capacitive coupling while achieving the desired inductance value [18]. As mentioned earlier the ASITIC EM solver tool was used to design an octagonal coplanar spiral 1.99nH inductor with Q = 8.7 at 5.7 GHz including interconnects (without interconnects the Q~10). The octagonal inductor and its passive lumped model are shown in Figure 5-6.

5.3. Mixer Noise Considerations

Mixer noise has been discussed in detail in Chapter 3.3. Chapter 5.1 also discusses a method for reducing 1/f or flicker noise in current sources for the proposed CDBQSHM mixer implementation. The sub-harmonic mixer design takes into account both thermal noise of the active devices, which is inversely proportional to bias current and is broadband, and flicker noise, which is present in the IF baseband. For low power design the bias current is limited and the only way to minimizing thermal noise is to reduce the number of devices and maximize gain under the limited gain conditions. This generally means larger device geometry to maximize transconductance. Generally the mixer output load is a filter, which has impedance near 800Ω to 1200Ω. For maximum power transfer the output of the mixer must also have large impedance which contributes significantly to mixer thermal noise. An active load can be used instead of a passive resistor, however, this has adverse effects on mixer linearity. This is one reason why the mixer noise figure is generally high, over 10 dB in most designs [5], [6], [13], [14].

The proposed sub-harmonic mixer architecture is designed to achieve low noise figure in a current limited environment. The mixer architecture has low active device count, and therefore, contribution of both thermal and flicker noise is reduced. The LO generation transistor pair works in the linear region the flicker noise contribution is less. Furthermore, use of inductors for mixer transconductance linearization contributes very low thermal noise and the current sources are designed for both low thermal and flicker noise. Additionally, to improve power supply rejection ratio (PSRR) large supply to ground capacitors are used and a low pass filter is used on all voltage bias nodes to reduce high frequency noise in mixer. Additionally the flicker noise of the current source is seen at the IF port of the mixer near the zero crossing of the applied LO signal. If the slew rate of the LO signal is kept high then *1/f* contribution can be minimized.

5.4. Sub-Harmonic Mixer Layout

The proposed sub-harmonic mixer is a double balanced mixer where symmetry is essential. Asymmetry gives rise to even order distortions including DC offsets so in layout utmost care is taken to make everything symmetric and balanced. Device matching is also critical and therefore layout uses highly matched passive like MIM capacitors, poly resistors, and uses multi-fingered active devices for RF matching. The active devices are placed in common centroid configuration to minimize mismatch due to process gradients in fabrication as shown in Figure 5-7. Also the transistors uses dummy poly gates and the load resistors have dummy resistors to improve matching. Figure 5-8(a) shows a custom drawn multi-fingered RF-FET layout. The Figure 5-8(b) shows the RF model for transistor in Figure 5-8(a).

Multi-fingered transistors are used with large number of contacts to achieve low gate, source, and drain resistance and also for realizing low parasitic capacitance. The source and drain area is enlarged to accommodate increased number of contacts for lowering drain and source

resistance. Lowered resistance translates to low power loss and reduced thermal noise. The mixer is designed to operate in the 5 to 6 GHz range where the wavelength of the RF signal is comparable to layout size so layout also implements on chip 50Ω microstrip transmission lines for high frequency RF and LO signals to contain the electro-magnetic (EM) radiation between interconnects improving port-to-port isolation and reducing unwanted coupling. Additional isolation is also achieved with use of local multiple signal grounds in the physical layout.

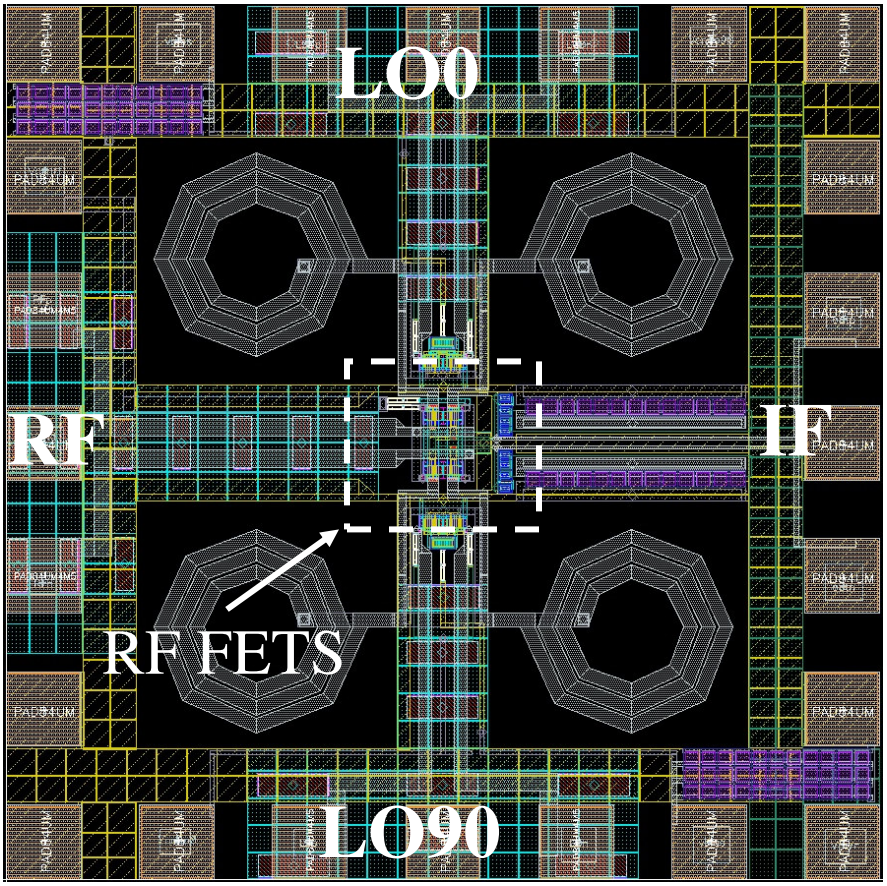
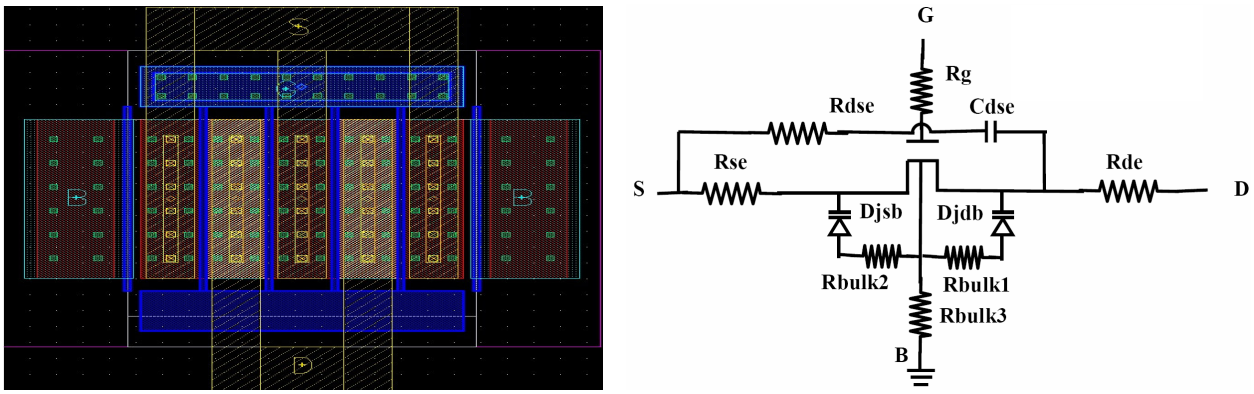


Figure 5-8. Sub-Harmonic mixer layout

While the layout in Figure 5-7 uses four degeneration inductors, the sub-harmonic mixer can be designed using two center-tapped inductors and in doing so can reduce the silicon real-estate by factor of two. Figure 5-9 shows the micrograph of two sub-harmonic mixer designed in TSMC 0.25-µm technology node.



(a) (b)

Figure 5-9. (a) NMOS RF FET layout and (b) RF Model for FET in (a)

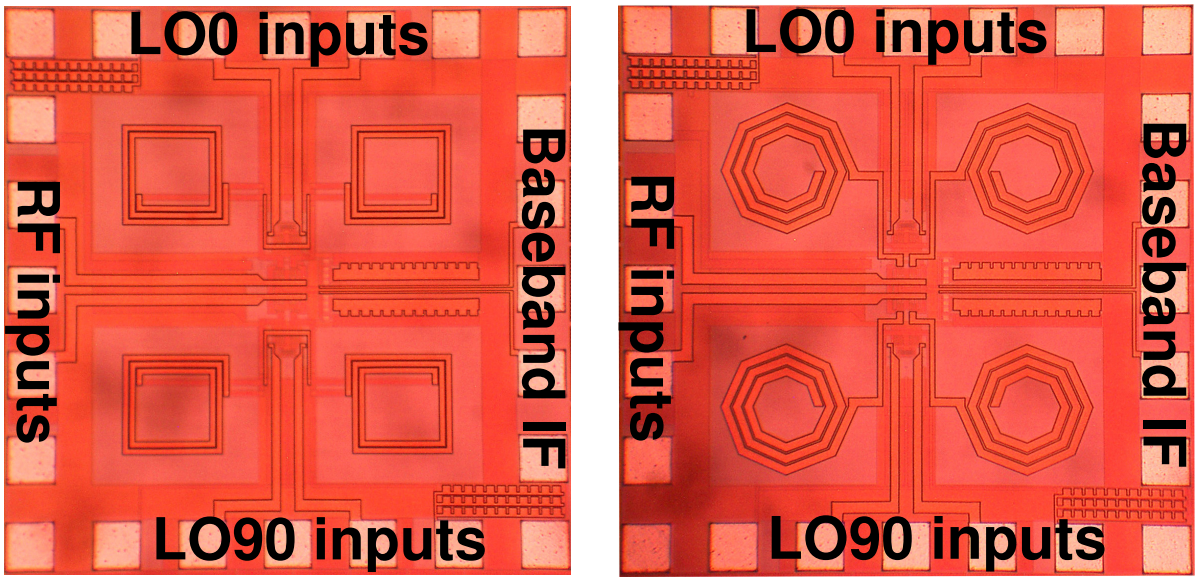


Figure 5-10. Micrograph of Sub-Harmonic mixer with (a) rectangular and (b) octagonal series feedback inductors [<1mm^2]

5.5. Sub-Harmonic Mixer Test Board and Instrumentation

The sub-harmonic mixer requires matching and DC blocking or bypass capacitors for proper biasing, which are generally large and are application dependent. For DCR front-end integration, inter-stage matching between the LNA and the mixer can be non-50Ω. For testing purposes the mixer requires external components including surface mount baluns to convert

single ended signals to differential, blocking capacitors, and a baseband unity power gain buffer (MAX4145), a phase trimmer or shifter and an attenuator. An external balanced phase shifter was used to generate 0^o and 90^o phases and a surface mount balun was used to generate 180^o and 270^o phases required for the LO generation. A passive coaxicom phase trimmer was used for LO phase and the attenuator is used to balance phase and amplitude within design specifications to minimize external mismatch that can be detrimental to IIP_2 performance, respectively. Figure 5-10 shows the test board setup for sub-harmonic mixer.

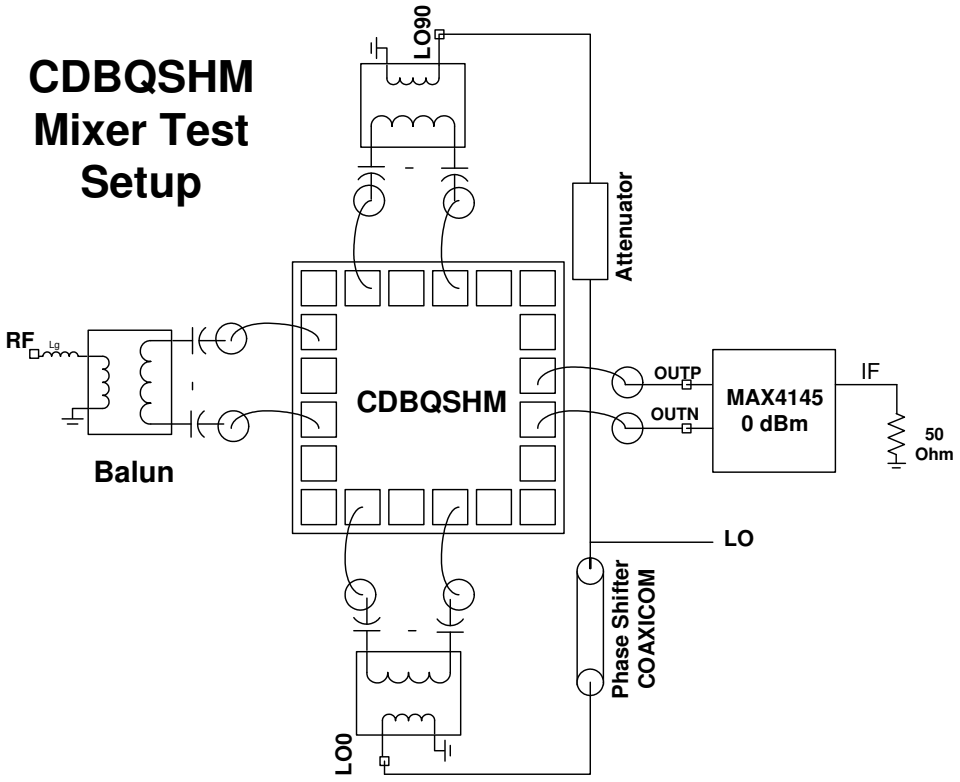


Figure 5-11. Test setup for Sub-Harmonic mixer measurement

The CDBQSHM mixer is manually wire bonded down to two-layered gold plated Rogers 3003 PCB characterization board, which has low skin effect losses at high frequencies. Figure 5-11 shows the mounted CDBQSHM on a test board and Figure 5-12 shows the laboratory setups for measurements.

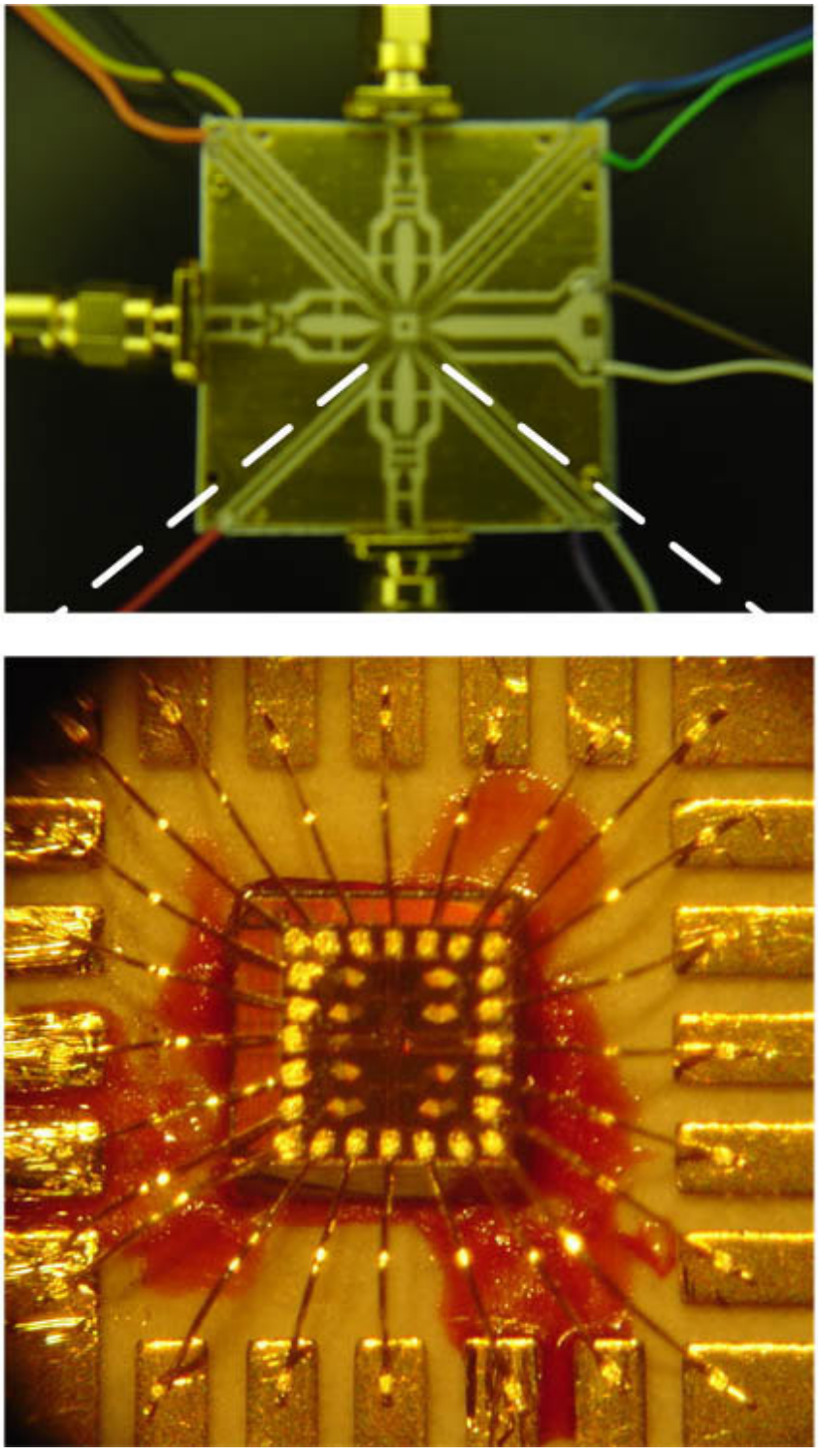
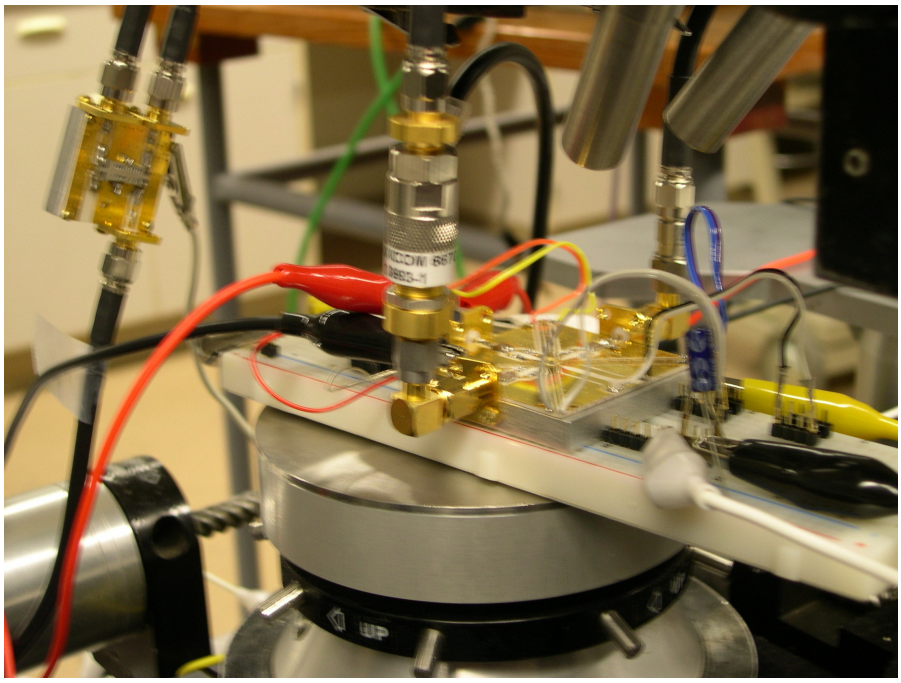
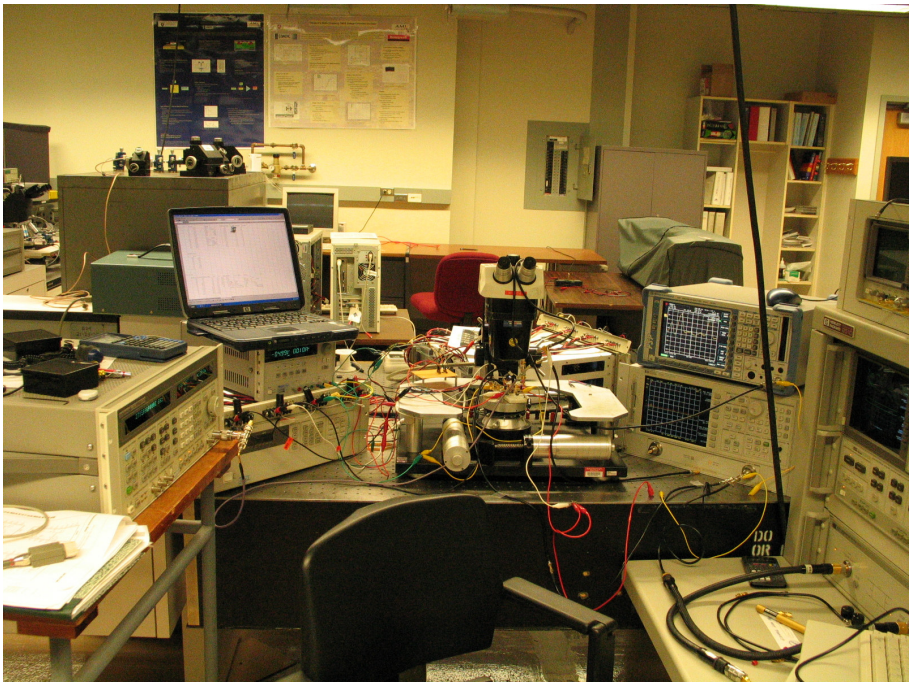


Figure 5-12. Mixer mounted on and manually wire-bonded to Rogers 3003 PCB characterization board



(a)



(b)

Figure 5-13. Laboratory setup for Sub-Harmonic mixer measurement

5.6. Sub-Harmonic Mixer Simulation and Measured Results

The CDBQSHM was implemented in the TSMC 0.25-µm digital CMOS process. The circuit simulation was done using the SPECTRE RF simulation suite. Table 5-1 summarizes the measured and simulated performance of the proposed CDBQSHM mixer.

Table 5-1: Summary Of CDBQSHM Performance

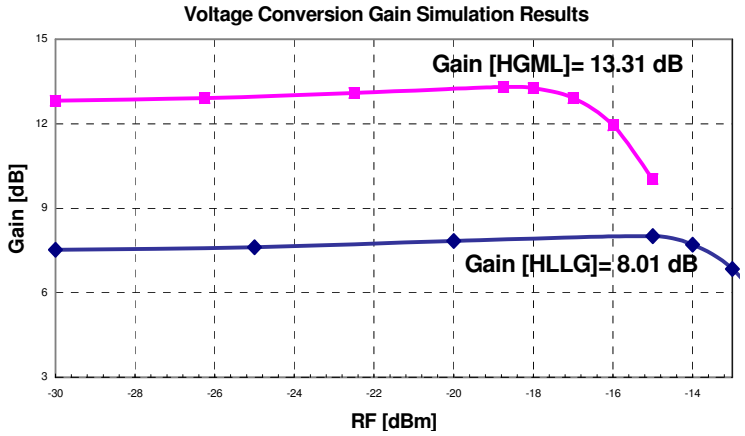
Performance Parameter	Simulated	Measured
CDBQSHM Versions	**HLLG**	**HLLG**
RF Frequency	5.6 GHz	5.6 GHz
LO Fundamental Frequency	2.8 GHz	2.8 GHz
Current from 3V Supply	1.75 mA	1.35 mA
Voltage Conversion Gain	8.01 dB	8.2 dB
P1dB	–12 dBm	–8 dBm
IIP3*	–6.5 dBm	–2.5 dBm
IIP2*	55.3 dBm	*36*+
DSB NF	5.96 dB	*TBM*
LO Power	0 dBm	0 dBm

Digital FETs were initially used, instead of manually created RF FETs since accurate models do not exist for the RF layouts. A first order mathematical model with gate, source and drain resistances was integrated with the digital model for simulations. However, the first order approximation results varied by less than 2% from the standard model and thus for the full set of mixer simulations standard TSMC provided FET models were used. Figure I in the Appendix I shows one of the sub-harmonic mixer simulation testbed.

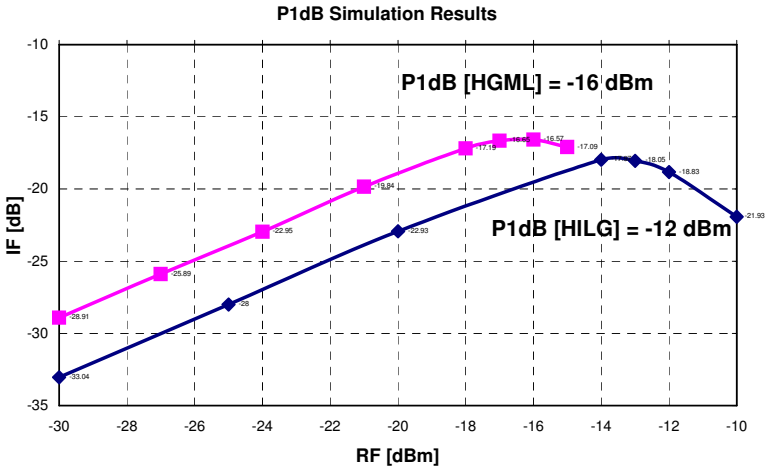
Originally two versions of CDBQSHM were designed; one targeting high gain (HGML) and the other high linearity (HLLG). Figures 5-14 (a) and 5-14 (b) show the gain and P_{1dB} plots for HGML and HLLG versions of sub-harmonic mixer, respectively. The difference is

* Simulated with 1% g_m mismatch, 0.5% R_L mismatch in the mixer circuit, and 2º of LO phase mismatch.
+ Measured IIP_2 with LO power of 0dBm. The IIP_2 performance of the sub-harmonic mixer is currently limited by instrumentation. The IIP_2 performance is expected to be better with improved measurement setup.

in the size of the degeneration inductors, which is the prime mechanism in gain and linearity tradeoffs. As mentioned in Chapter 5.2, the HLLG version was selected for its linearity. The input matching network for RF port of sub-harmonic mixer with rectangular inductor consisted of a 2.5 nH inductor in series with a bypass capacitance of 5.6 pF to achieve input return loss of –25 dB.



(a)

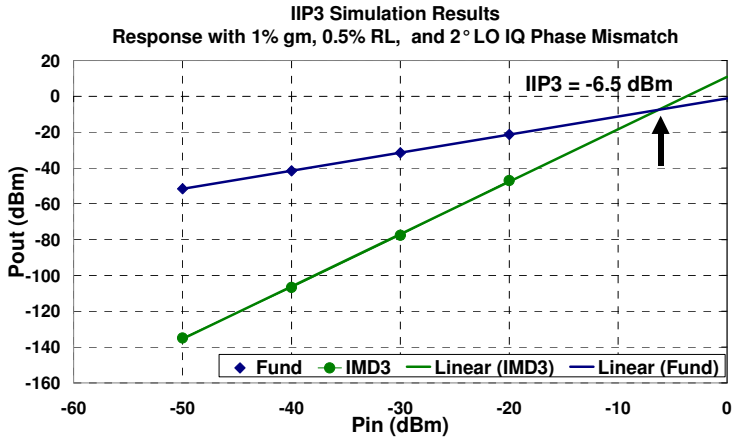


(b)

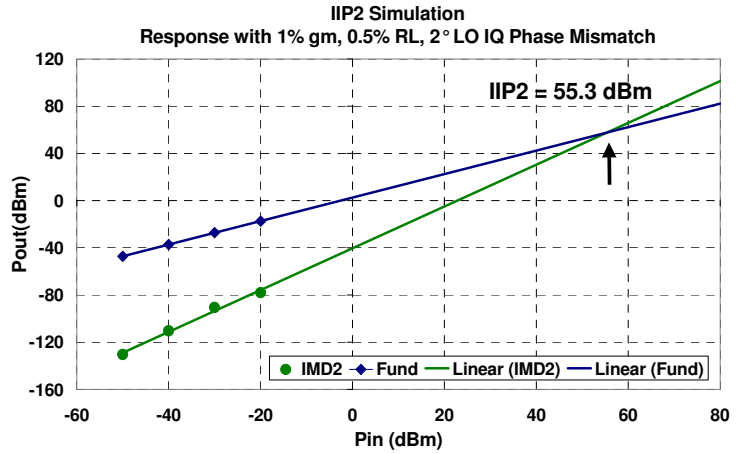
Figure 5-14. (a) Gain and (b) P_{1dB} compression for HGML and HLLG versions of CDBQSHM

For HLLG mode the simulated conversion gain is 8.01 dB and P_{1dB} is –12 dBm. A two-tone test was applied to measure the other linearity performance barometers including IIP_3 and IIP_2. The CDBQSHM simulations shows –6.5 dBm of IIP_3 achievable and as expected a high

IIP_2 of 55.3 dBm measured even with inclusion of 1% g_m mismatch, 0.5% R_L mismatch in the mixer circuit, and 2º of LO phase mismatch (see Figure 5-15). These mismatches were included in the simulation to simulate the worst-case non-ideal conditions for the mixer. The proposed sub-harmonic mixer architecture, therefore, is suitable for DCR applications where IIP_2 greater than 40 dBm is desired.



(a)



(b)

Figure 5-15. The CDBQSHM simulated (a) IIP_3 and (b) IIP_2 performance.

The measured results show good correlation with simulated results but with some improvements in linearity while consuming less current. The measurement results are summarized along with the simulated results in Table 5-1. Figure 5-16 shows a comparison of

simulated and measured voltage conversion gain. The mixer is able to achieve measured voltage conversion gain 8.2 dB and P_{1dB} of –8 dBm. The measured results show 4 dB improvement in P_{1dB} while the conversion gain of the mixer compares very well with simulated results of 8.01 dB. A two-tone test with spacing of 1.5 MHz was done to measure IIP_3 and IIP_2 with frequency

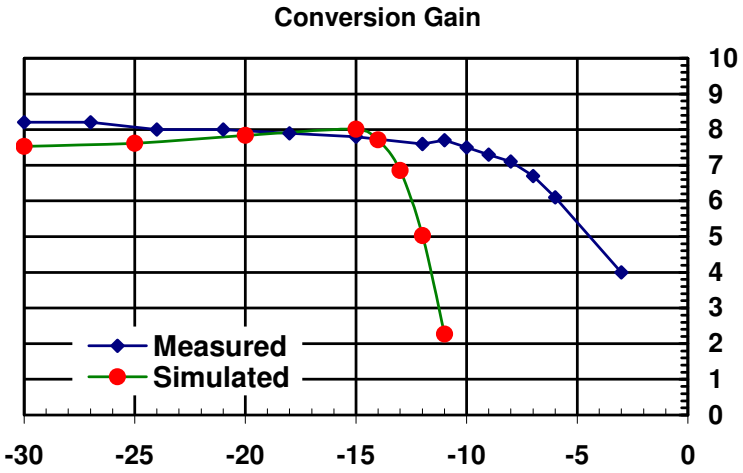


Figure 5-16. The measured and simulated conversion gain and P_{1dB} for CDBQSHM.

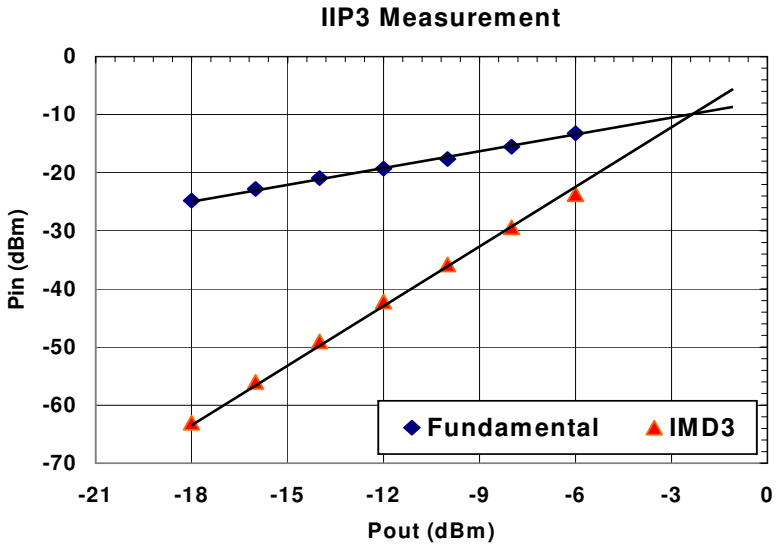
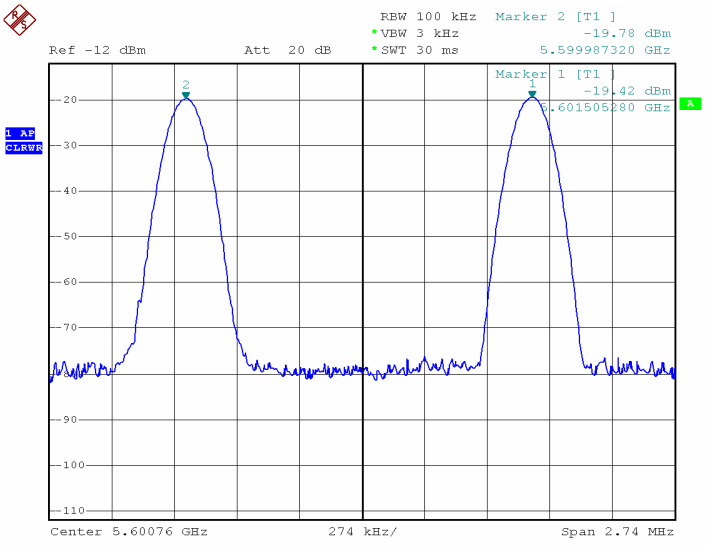


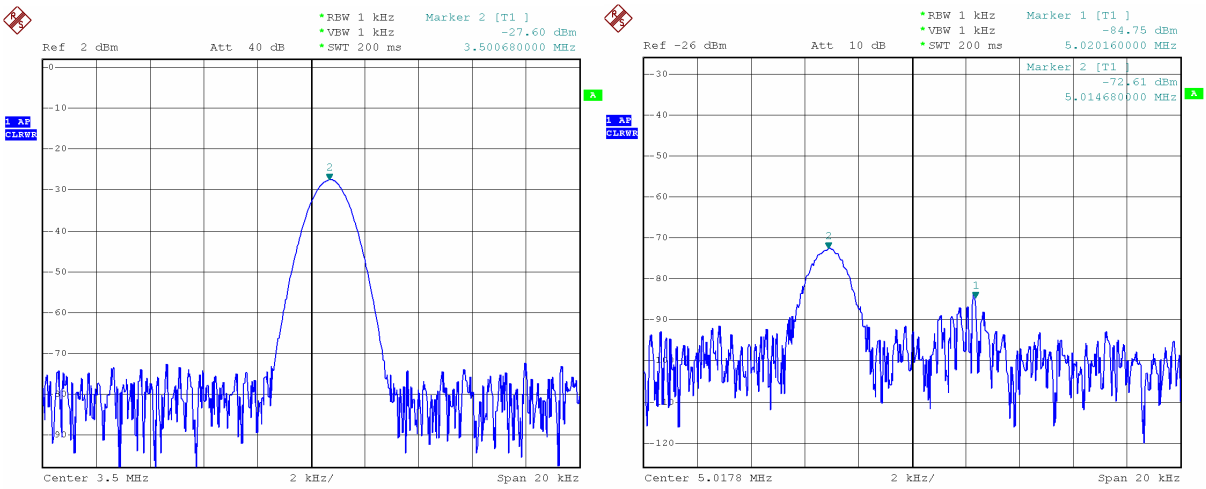
Figure 5-17. The measured IIP_3 performance shows 4 dB improvements over simulation.

tones at 5.6 GHz and 5.6015 GHz, respectively. The LO frequency is set at 2.799 GHz such that the LO frequency will be generated in the sub-harmonic mixer at 5.598 GHz. The resultant IF tones are at approximately 2 MHz and 3.5 MHz, respectively. Figure 5.18(a) shows the RF two-

tones and Figure 5.18(b) shows the resultant down converted signal at IF with 3rd order intermodulation shown in 5.18(c).



(a)



(b) **(c)**

Figure 5-18. A two-tone test to measure IIP_3 (a) Input tones at 5.6 GHz and 5.6015 GHz (b) One of the IF tone at 3.5 MHz (c) IMD_3 peaks at 5 MHz

The 3rd order intermodulation distortion, IMD_3, can be seen at $2\omega_1 \pm \omega_2$ and $2\omega_2 \pm \omega_1$ (see Table 3-2). This means for IF tones at 2 MHz and 3.5 MHz an IMD_3 tone should be seen at

0.5 MHz and 5 MHz. For example for the measurement in Figure 5-18, we can calculate the IIP_3 at a particular input power by using Eq. (5.7), which is derived from Figure 3-4,

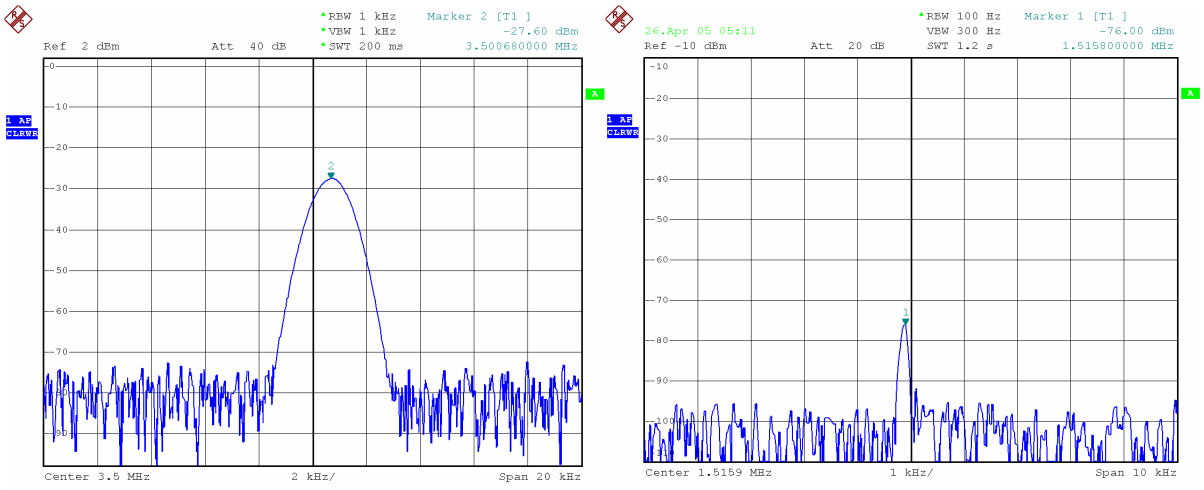
$$IIP_3 = \frac{P_{out} - P_{IMD_3}}{2} + P_{in} \tag{5.7}$$

$$IIP_3 = \frac{-27.63dBm - (-72.63dBm)}{2} + (-25dBm) = -2.5dBm \tag{5.8}$$

to get the measured IIP_3 for the sub-harmonic mixer of –2.5 dBm. The RF signal losses, due to assembly, of 5 dBm is assumed and is accounted for in the example given in Eq. (5.8). The measured IIP_3 extracted from different input power values is approximately –2.5dBm for CDBQSHM is shown in Figure 5-17. The IIP_3 also reflects the 4 dB improvements in P_{1dB} as the measured IIP_3 of –2.5 dBm is an improvement over simulated –6.5 dBm. The improvement is primarily due to manual layout of digital FETs to improve on the RF performance, which, was not modeled in the circuit simulation.

Similar to IIP_3 measurement using two-tone test we can also extract the IIP_2 value for the sub-harmonic mixer. The 2nd order intermodulation distortion, IMD_2, can be seen at $\omega_1 \pm \omega_2$ and $\omega_2 \pm \omega_1$ (see Table 3-2). This means for frequency tones at 5.6 GHz and 5.6015 GHz an IMD_2 tone of interest should be seen at 1.5 MHz. Figure 5-19 shows the IMD_2 response to two-tone test and Figure 5-20 shows the corresponding IIP_2 value for the CDBQSHM. The measured IIP_2 of 36 dBm is less than simulation value of 55.3 dBm shown in Figure 5-14(b). The measured IIP_2 for the sub-harmonic mixer are limited by the measurement setup. For proper IIP_2 measurement, the simulation conditions for amplitude and phase mismatch must be satisfied. However, in actual measurement it is very difficult to verify if externally provided LO amplitude and phases are within the limits used in simulation. The commercial coaxicom phase trimmer or shifter phase steps accuracy is not good enough at 2.8 GHz to properly set the LO phase below

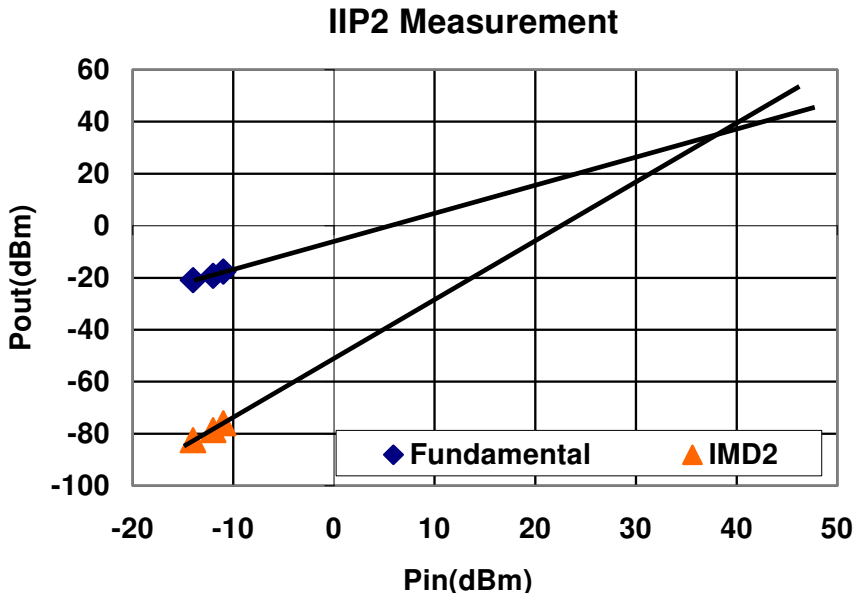
2° as simulated. Furthermore, the commercial surface mountable baluns used in the characterization board has phase inaccuracy of ± 5° and amplitude inaccuracy of ± 0.4 dB. Therefore, it is difficult to say if the IIP_2 performance measured is that of the mixer or is limited by the test setup. Even with the current setup, however, the measured IIP_2 value of 36 is relatively good and is at or over the level of Gilbert cell mixers [5], [6], [13], [14]. With a verifiable test setup for the sub-harmonic mixer we can confident the mixer can achieve higher IIP_2 similar to simulation. Further efforts are needed to improve on the setup and we expected the IIP_2 results to be close to or better than simulated values where, the mixer achieves high IIP2 value of 55.3 dBm even under intentional worst case 1% gm mismatch, 0.5% R_L mismatch in the mixer circuit and 2º LO fundamental phase mismatch scenario. The IIP_2 also varies with input LO fundamental power level as shown in Figure 5-20 (b) achieving maximum IIP2 of 38 dBm for 1 dBm of LO power. Larger LO amplitude may suppress the amplitude mismatch in the LO port of the mixer, however, as measurement shows there is a limit to how much the LO power can be increase to improve the IIP_2.



(a) **(b)**

Figure 5-19. A two-tone test to measure IIP2 (a) One of the IF tone at 3.5 MHz (b) IMD2 peaks at 1.5 MHz.

The simulated 5.96 dB double side band noise figure (DSB NF) for the CDBQSHM is very good for any CMOS mixer and is better than already published sub-harmonic mixer architectures [5],[6],[13],[14]. Due to lack of necessary equipment, the noise figure of the mixer has yet to be measured



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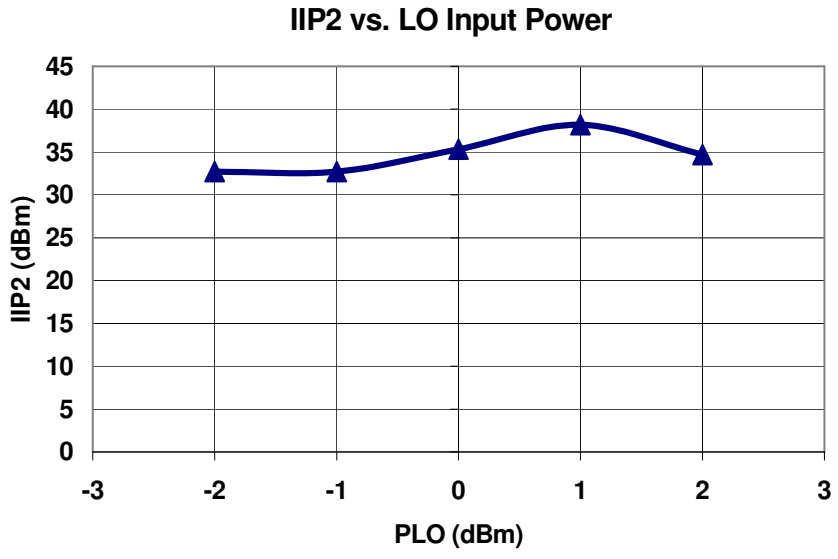


(b)

Figure 5-20. A two-tone test to measure IIP_2 (a) Input tones (without compensation for assembly loss) (b) One of the IF tone at 2 MHz (c) IMD_3 peaks at 1.5 MHz

6.0. FUTURE RESEARCH AND DIRECTION

For a system-on-a-chip (SoC) solution, the RF and analog circuits must scale with its digital counterpart for a low-cost highly integrated solution. This means low voltage and small silicon real estate RFICs are needed. The low supply voltage means low dynamic range for RF and analog circuits especially at high frequency while low silicon real estate requires inductor-less solutions. Therefore, the earlier methods for linearization described in Chapter 5.2 utilizing series feedback become more challenging for RFICs. Commonly, a series feedback method using inductor or resistive degeneration is used to improve the linearity of the mixer, however, this solutions is not very ideal due to its silicon real estate requirements, linearity/gain trade-offs, and noise. A novel CMOS inductor-less sub-harmonic mixer (CSHM), which utilizes a bias-offset transconductance (g_m) linearization technique, is proposed to achieve high linearity and high performance while occupying very low silicon real estate [19].

6.1. A Novel Low Voltage Inductor-less Sub-Harmonic Mixer

The bias offset transconductance linearization approach uses two parallel FETs in order to minimize the effect of 3rd and higher order non-linearity effects. This can been seen by first modeling the nonlinear I_{DS}-V_{GS} relationship of a FET by means of taylor series expansion around a particular V_{GS} bias point as follows:

$$i_{ds}(t) = g_{m1} v_{gs}(t) + g_{m2} v^2{}_{gs}(t) + g_{m3} v^3{}_{gs}(t) + \ldots \tag{6.0}$$

where,

$$g_{m1} = \frac{dI_{DS}}{dV_{GS}}\Big|_{V=V_{GS}};\ g_{m2} = \frac{1}{2!}\frac{d^2 I_{DS}}{dV^2{}_{GS}}\Big|_{V=V_{GS}};$$

$$g_{m3} = \frac{1}{3!}\frac{d^3 I_{DS}}{dV^3{}_{GS}}\Big|_{V=V_{GS}};\ etc. \tag{6.1}$$

$$v_{gs}(t) = V_A(\cos w_1 t + \cos w_2 t) \tag{6.2}$$

Substituting two frequency tones in Eq. (6.1), commonly referred as the two tone test, into (6.1) will result in generation of odd and even order intermodulation products that include the 2nd and 3rd order intermodulation terms, IMD_2 and IMD_3,, respectively . The magnitude of IMD_3, the distortion due to 3rd order effects in the case of transconductance, g_{m3}, can be expressed by computing the ratio of non-linear current at 3rd order intermodulation frequency, i_{ds} $(2w_1\text{-}w_2)$ and at fundamental frequency, i_{ds} (w_1) and is shown in Eq. (6.3).

$$IMD_3 = \left|\frac{i_{ds,(2w1-w2)}}{i_{ds,w1}}\right| = \left|\frac{\frac{3}{4} gm_3 V_A^3 + \frac{25}{8} gm_5 V_A^5}{gm_1 V_A + \frac{9}{4} gm_3 V_A^3 + \frac{25}{4} gm_5 V_A^5}\right| \tag{6.3}$$

From Eq. (6.3) we can see that to reduce the 3rd order distortion the odd order terms should be minimized. Usually the 5th order terms are small and can be neglected in analysis. Therefore, for high linearity we focus primarily on 2nd and 3rd order distortion. It is clear from the analysis that if we can eliminate or reduce the g_{m3} term, the IIP_3 (3rd order input intercept point) can be maximized or the IMD_3 minimized. A bias offset techniques using two parallel FETs as shown in Figure 6-1 is applied to do just that, i.e, reduce g_{m3} term at the bias of interest in the mixer RF port to achieve high linearity [19],[20].

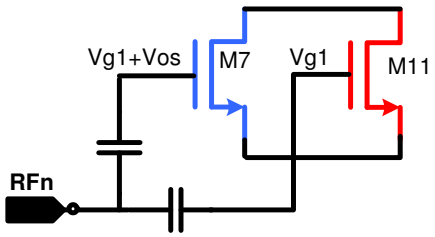
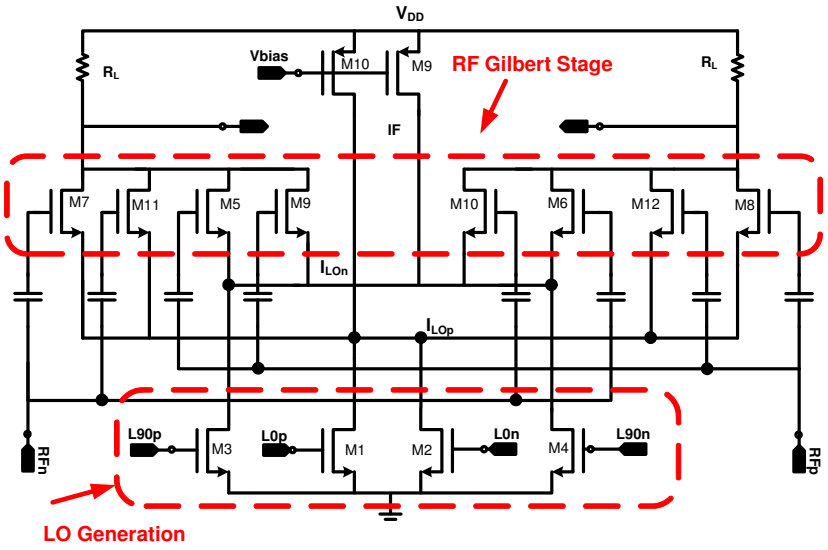


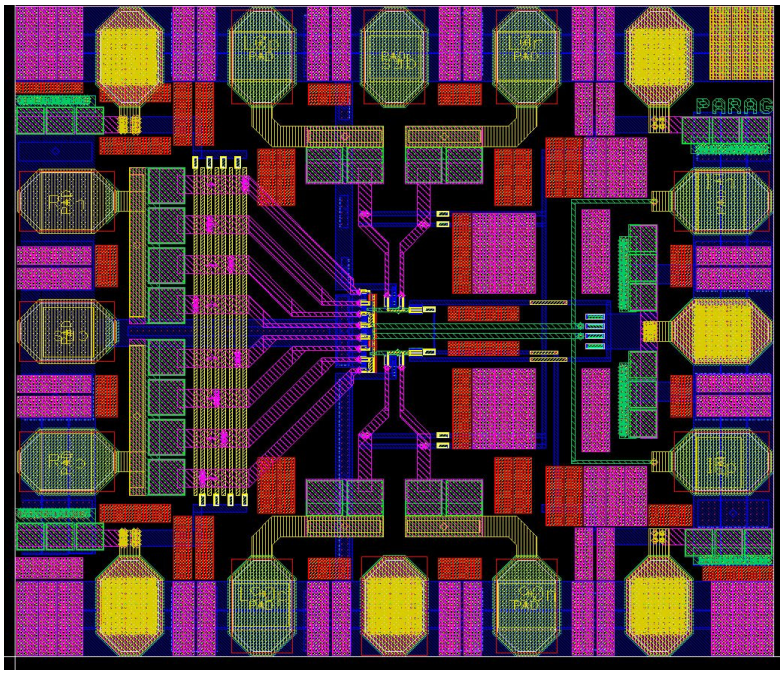
Figure 6-1. Bias Offset circuit implementation in Gilbert stage using two FETs

A novel highly integrated 5.6 GHz inductor-less doubly balanced sub-harmonic mixer using *½ X* LO generation scheme in Figure 6-2, in which LO fundamental frequency is half that

of the RF, is proposed. The proposed low power mixer architecture achieves high linearity using a bias-offset transconductance linearization technique avoiding commonly used series feedback inductor, thus, significantly reducing the silicon real estate [18].



(a)



(b)

Figure 6-2. (a) Simplified schematic of the proposed 5.6 GHz inductor-less sub-harmonic mixer (CSHM) with gate bias network not shown (b) layout of CSHM in (a).

The simulated performance of the CSHM is tabulated in Table 6-1. The mixer achieves IIP_3 of 0 dBm, conversion gain of 8.05 dB and IIP_2 of 45 dBm while consuming only 2.6 mA from a 1.8V supply. Details of CSHM design can be found in [19].

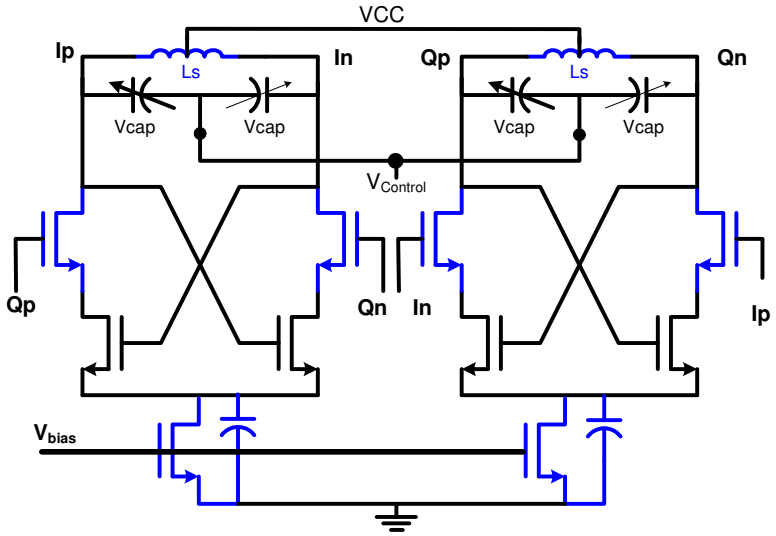
Table 6-1: Summary of Low Voltage Inductor-less CSHM Performance

Performance Parameter	Simulated Results
RF Frequency	5.6 GHz
LO Fundamental	2.8 GHz
Current from 1.8V Supply	2.6 mA
Voltage Conversion Gain	8.05 dB
IIP_3	0 dBm
IIP_2 (w/ 0.5% mismatch)	45.3 dBm
P_{1dB}	– 13.5 dBm

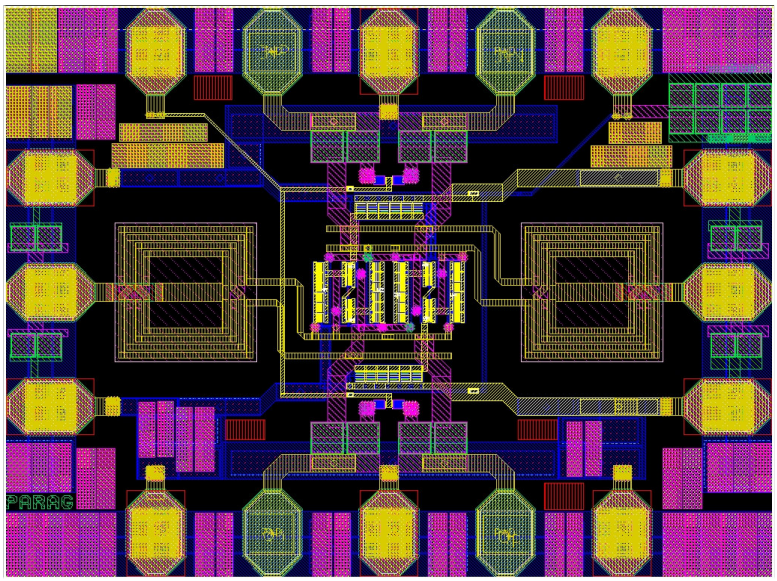
6.2. A Low Voltage Quadrature LC VCO for LO Generation

A voltage-controlled oscillator is used to generate I/Q (quadrature) LO signals required in the sub-harmonic mixer and is another critical component of the DCR receiver since its limitation can adversely affect the DCR performance in terms of data bandwidth, intermodulation. A new low voltage cascode quadrature LC VCO (CQ) architecture as in Figure 6-3 can be used. The CQ VCO has lower *1/f* noise characteristic since the cascode phase coupling transistor primarily operates in linear region where *1/f* noise is low which means low phase noise [21]. In addition to improved quadrature phase noise, the architecture can also achieve lower phase error without much trade off with the phase noise. The cascode quadrature LC VCO can be used with a 4 way center-tapped differentially coupled inductor, as shown in Figure 2-7(b), to achieve high phase noise while operating below 1.5 V supply voltage. Simulation shows that even with the two-way center tapped inductors, as shown in Figure 6-3 (b), the CQ VCO is able to achieve phase noise of *–116 dBc/Hz* at *1 MHz* frequency offset while

maintaining the phase error within 1^{o}. The CQ VCO operates at 1.35 V and consumes 8.9 mA of quiescent current. When 4-way center-tapped inductors, which have lower parasitic series resistance, are implemented the phase noise is expected to improve further.



(a)



(b)

Figure 6-3. (a) Simplified schematic of the proposed Cascode Quadrature LC VCO (CQVCO) and (b) layout of CQ VCO in (a) using 2-way center-tapped inductors.

7.0. FINAL THOUGHTS AND CONCLUSIONS

This thesis is a culmination of work for designing the front-end of a direct conversion receiver (DCR) in the 5 GHz ISM frequency Band. This work gives an overview of direct conversion RF transceiver architecture and its design challenges and potential solutions for addressing 1/f noise, DC offset, 3rd order intermodulation products and more importantly 2nd order intermodulation. A novel CMOS doubly balanced quadrature sub-harmonic mixer (CDBQSHM) is demonstrated The CDBQSHM has high immunity to 2nd order intermodulation products and achieves high IIP_2 needed for DCR applications. While sub-harmonic are generally associated with microwave frequency design in 10s and 100s of gigahertz, a novel topology shows its viability for 5 GHz ISM band applications, which includes 802.11a and Hiperlan2 wireless LAN standards in the US and Europe, respectively. The design emphases trifecta of low power, low voltage, and low cost sub-harmonic mixer design that can be applied in CMOS and SiGe technology. Two improved mixers address design of low voltage RFICs with high dynamic range overcoming voltage headroom issues generally associated with high-speed analog and RF circuits.

In summary, a new low power and high IIP_2 0.25-μm CMOS doubly balanced sub-harmonic mixer for 5 GHz Industrial Scientific Medical (ISM) band direct conversion - zero IF receiver was optimally designed, simulated, fabricated and tested. Using *½ X* LO frequency generation scheme, based on a voltage to current frequency doubler LO generation technique, the sub-harmonic mixer overcomes LO self-mixing problem common in conventional direct conversion receivers (DCR). Measurement shows the sub-harmonic mixer is able to achieve voltage conversion gain of 8.2 dB, input compression, P_{1dB} of –8 dBm, IIP_3 of –2.5 dBm, and IIP_2 of 36 dBm while consuming only 1.35 mA of DC current. Measured results correlate well

with simulated results where with 1% g_m mismatch, 0.5% load mismatch and 2º LO phase error the mixer is able to achieve high IIP_2 of 55.3 dBm, IIP_3 of –6.5 dBm, and voltage conversion gain of 8 dB. The proposed mixer takes up less than $1mm^2$ of silicon real estate including test die pads. A Novel low voltage sub-harmonic mixer using bias offset transconductance linearization technique is also introduced with mixer core only occupying less than $0.3mm^2$. Furthermore, a low voltage cascode LC VCO is introduced for quadrature phase generation required in the sub-harmonic mixers. The mixer theory developed and discussed in the thesis agrees with simulation and the measurement data and can be used as a design guide for developing high performance mixer circuits for many applications including superheterodyne transceivers and are not just limited to homodyne transceivers.

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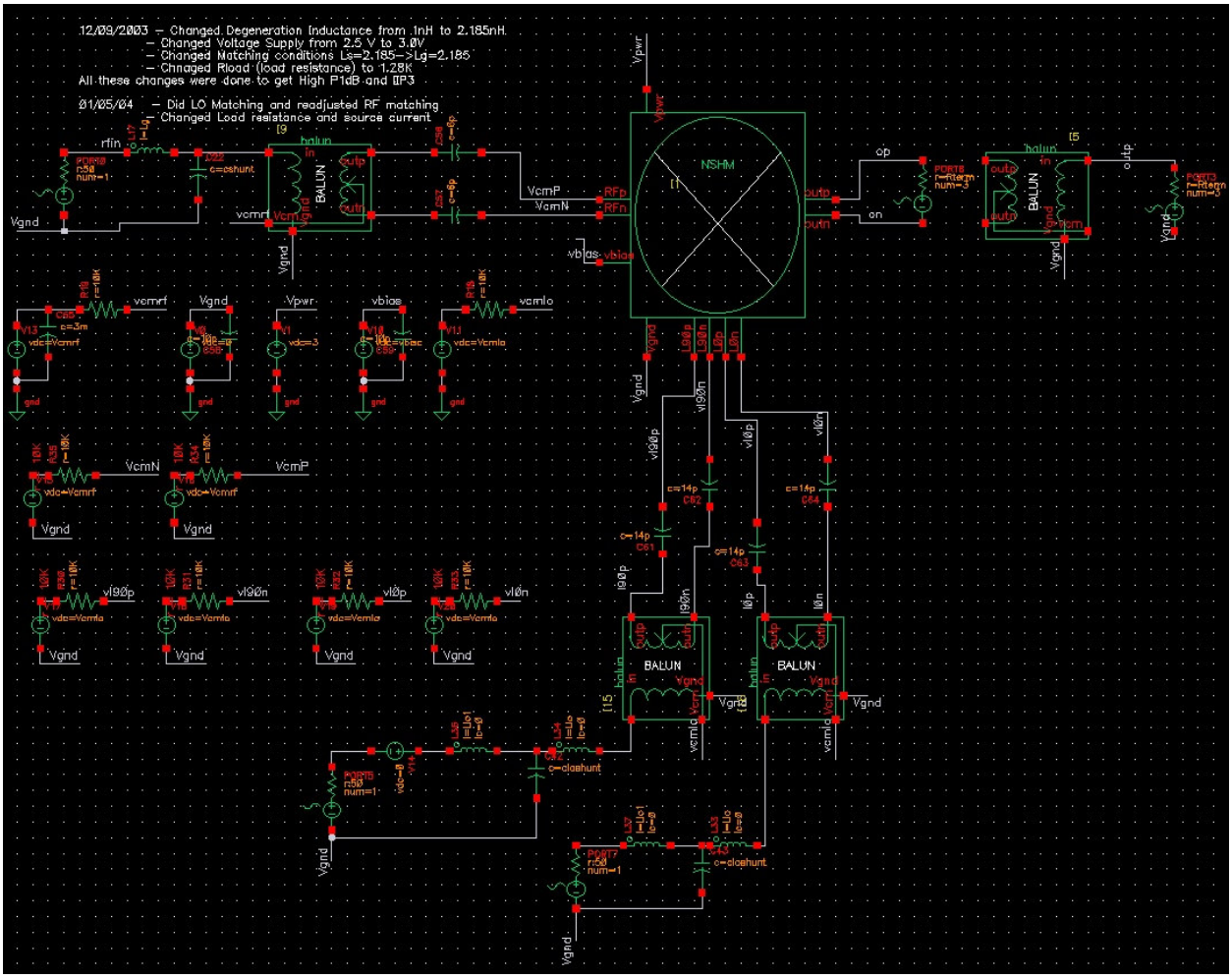
AUTHOR'S BIOGRAPHICAL SKETCH

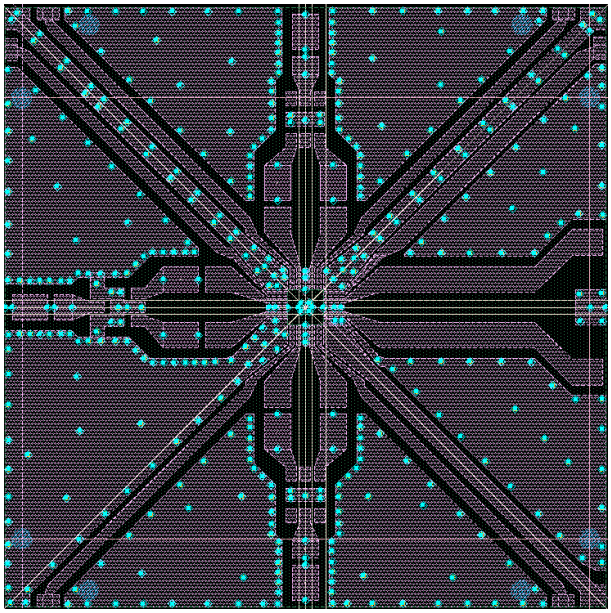
Parag Upadhyaya received the BSEE degree from Washington State University with distinction in 2000. He was with Cypress Semiconductor data communication division until 2003 as a design engineer where he specialized in high speed wired transceivers including development of OC48 system. Since 2003, he has been a MSEE student at Washington State University in the Advanced RF and Mixed-Signal Application Group (ARMAG). He authored or co-authored over 13 journal, conference, and book chapter publications. His current research interest includes wired and wireless transceivers and monolithic microwave integrated circuits (MMICs) for high-speed data communications.

APPENDIX I

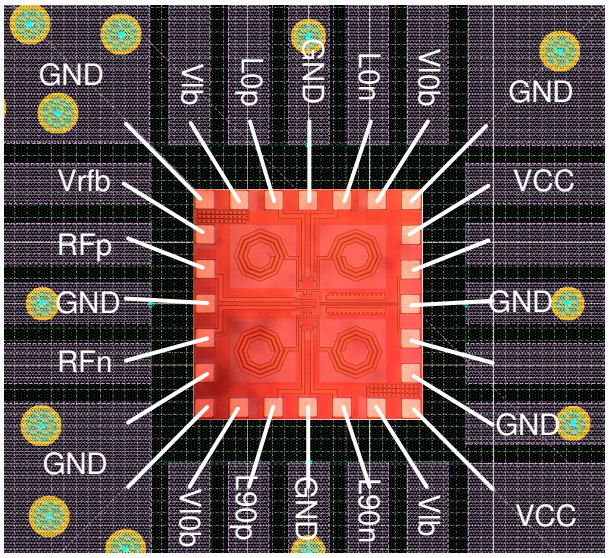
I. Mixer Simulation Test-Bed



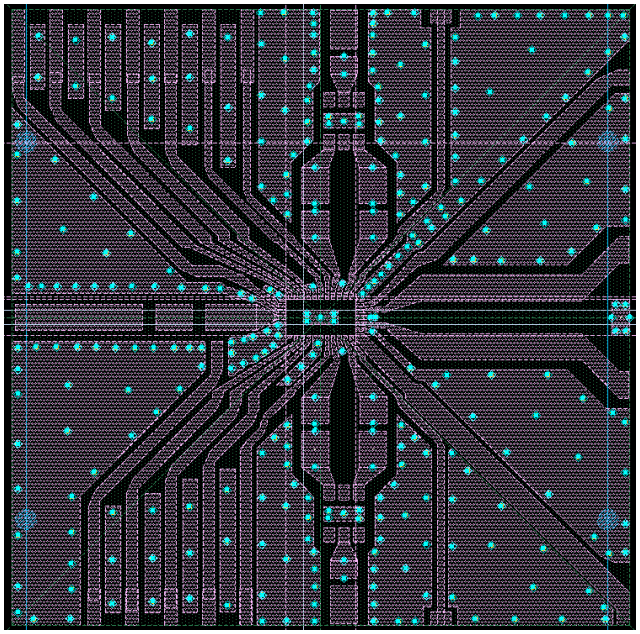
II. Mixer Characterization Board Layout



III. Symbolic Pin outs for Mixer on Characterization Board



IV. I-Channel DCR Characterization Board Layout



V. Symbolic Pin outs for I-Channel DCR