MODELING OF FETS WITH ABNORMAL GATE GEOMETRIES FOR RADIATION HARDENING

By

CORBIN LEIGH CHAMPION

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Chair

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MODELING OF FETS WITH ABNORMAL GATE GEOMETRIES FOR

RADIATION HARDENING

Abstract

by Corbin Leigh Champion, M.S.
Washington State University
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Chair: George S. La Rue

A new accurate modeling technique is described that provides a SPICE model, based on the SPICE model of a standard rectangular FET, for any FET with an abnormal gate geometry, such as an annular FET. The new model uses conformal mapping to map an abnormal geometry onto a rectangular geometry. Conformal mapping has been used as a tool for this type of problem in previous research, but the new method presented splits the problem into mapping of multiple regions defined by the equal-potential lines on the rectangular gate being inverse mapped onto the given gate geometry. The length of the equal potential lines are used to define the length of the channel in a region of the gate and the spacing of equal potential lines is used along with space-charge conservation to find how the output resistance is altered by the geometry. This method for finding accurate DC models of a FET with any gate geometry was then automated making it fast and easy to use. To get correct small-signal models, as well, the necessary changes to a BSIM3 SPICE model are described taking into account the effect of geometry on the

small-signal capacitance values. The modeling of the DC behavior is shown to be accurate to better than 10% for drain current values and 11% for output resistance. Capacitance measurements agree with theory to better than 8%. The models are proven to be accurate for annular FETs and for another radiation hardened FET, which is called a horseshoe FET. Other radiation hardened FETs are also described. These FETs include gate around source and gate around transistor FETs. The DC and small-signal models for these FETs were shown accurate to within 20% using a simplified modeling technique. The methods used to model these different types of FETs with abnormal gate geometries are very powerful allowing the modeling of transistors of any gate geometry with high accuracy, whether for radiation hardening or another purpose.

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Dedication

This thesis is dedicated to my parents for pushing me to do more and my fiancé for making everyday joyous and worthwhile.

SECTION ONE

INTRODUCTION

In space applications, high-energy physics experiments as well as other ionizing radiation environments, it is necessary to harden critical circuits to the effects of radiation or otherwise suffer reduced performance or complete device failure. This hardening can come from using a process that has been designed to be radiation hardened, (radiation hardening by process), or by using one of many non-standard transistor layouts and/or circuit topologies that reduce the effect of radiation on device performance (radiation hardening by design). Using radiation hardening by process often limits the designer to large minimum gate dimensions while at the same time greatly increasing the power consumption and cost of fabrication. These processes have lower speed devices and have lower yield than a standard process [1]. Instead, if radiation hardening by design techniques are used the negatives listed for radiation hardening by process do not arise, because state-of-the-art processes with small minimum gate lengths can be used. Devices with minimum gate lengths may not be tolerant to as high level of radiation, however.

These key differences between the two described ways of hardening are very important. For example, the speed of the devices can greatly limit the functionality of a system, such as the type and speed of communication available to a satellite designed in a radiation hardened process. Also for space missions, the power consumption can limit the duration of a mission or limit the mission by requiring longer recharge periods. For the reasons listed, radiation hardening by design is often the method chosen for hardening a circuit when possible.

Within radiation hardening by design, there are two methods for making a circuit hardened. A designer could choose a circuit architecture that is less susceptible to the effects of radiation or a designer could use non-standard, or abnormal, FETs with non-rectangular gate geometries to limit the effects of radiation. The first method can limit the designer's options, which can make it difficult to meet specifications for a given design, and there is often limited improvement in total-dose tolerance with this approach, while there can be significant improvement in single event upset (SEU) tolerance [2]. Also, this method typically involves creating an architecture that meets specifications in standard SPICE simulation and then running the design through a radiation effect simulator or having test chips subjected to radiation after fabrication. If the device fails in the radiation effect simulator or when tested with an ionizing radiation source, the designer must redesign the circuits that failed. The limitations imposed on the designer and of the effectiveness of this method by itself along with the strong possibility of increased design time and cost often leads designers to use the second method of radiation hardening by design, with or without the use of the first for SEU tolerance.

One main problem associated with the second method is that, if abnormal gate geometries, such as an annular gate, are used to harden FETs, complete and accurate models do not exist and instead rough approximations or data from test chips may be used by designers to create an initial layout [1],[3]. Unfortunately, rough approximations can cause multiple design iterations, because they may cause simulation to not match fabricated devices well. Also, if a test chip is designed to get higher accuracy models, the circuit design will be delayed because of the necessary design, fabrication and testing time necessary for the test chip before design can begin. This will also increase the cost

of the overall project. To meet this need for complete and accurate models, this thesis will present new methods for creating models and compare the simulations results using the new models to experimental data for several layouts with abnormal gate geometries that provide for radiation hardening. The list of transistors studied will include previously used layouts, as well as some novel designs for radiation hardening. The methods provided are very powerful and can be extended to be used for any gate geometry, including those not designed for radiation hardening.

SECTION TWO

MOTIVATION: EFFECTS OF RADIATION ON FETS

To appreciate better the purpose of and layouts used for radiation hardening by design, it is important to first understand what effects ionizing radiation will have on FET performance and how radiation causes these effects. The study of the effects of radiation on the behavior of FETs has been studied very thoroughly by previous works, but only the main issue and the cause of it will be discussed here [3],[4],[5],[6],[7]. The main cause of problems, associated with total-dose levels, with a rectangular gate FET come from the fact that ionizing particles passing through a semiconductor or an insulator creates electron-hole pairs [4]. The number of pairs created is simply proportional to the amount of energy deposited in the material by the ionizing radiation source. The electron-hole pairs created in the gate itself or in doped semiconductor material are of little importance as the pairs quickly disappear since the materials are of relatively low resistance. For oxides this is not the case. Gate or field oxide is an insulator and the mobility of the electrons and holes created are greatly reduced within them. The electrons and the holes behave quite differently. The mobility of electrons in an insulator can be higher than that of holes by five to twelve orders of magnitude [3]. As a result, if a positive voltage is put on the gate, nearby electrons will move into the gate in a very short period of time and recombine there. The holes instead will slowly move towards the substrate [4]. Some of the holes do not completely go into the substrate and recombine with electrons there, but will remain trapped at the oxide-substrate boundary. The number trapped will be proportional to the number of defects in the oxide [5]. These

trapped holes will remain even if there is no longer a gate voltage applied leaving a net positive charge trapped in this region. This positive charge in the gate or field oxide will attract a layer of electrons that will create a channel for n-channel devices, see Figure 2.1, after a sufficient dose of radiation has been applieed. This will have very little effect on the behavior of p-channel devices where the channel conducts holes[8]. Also, the gate of

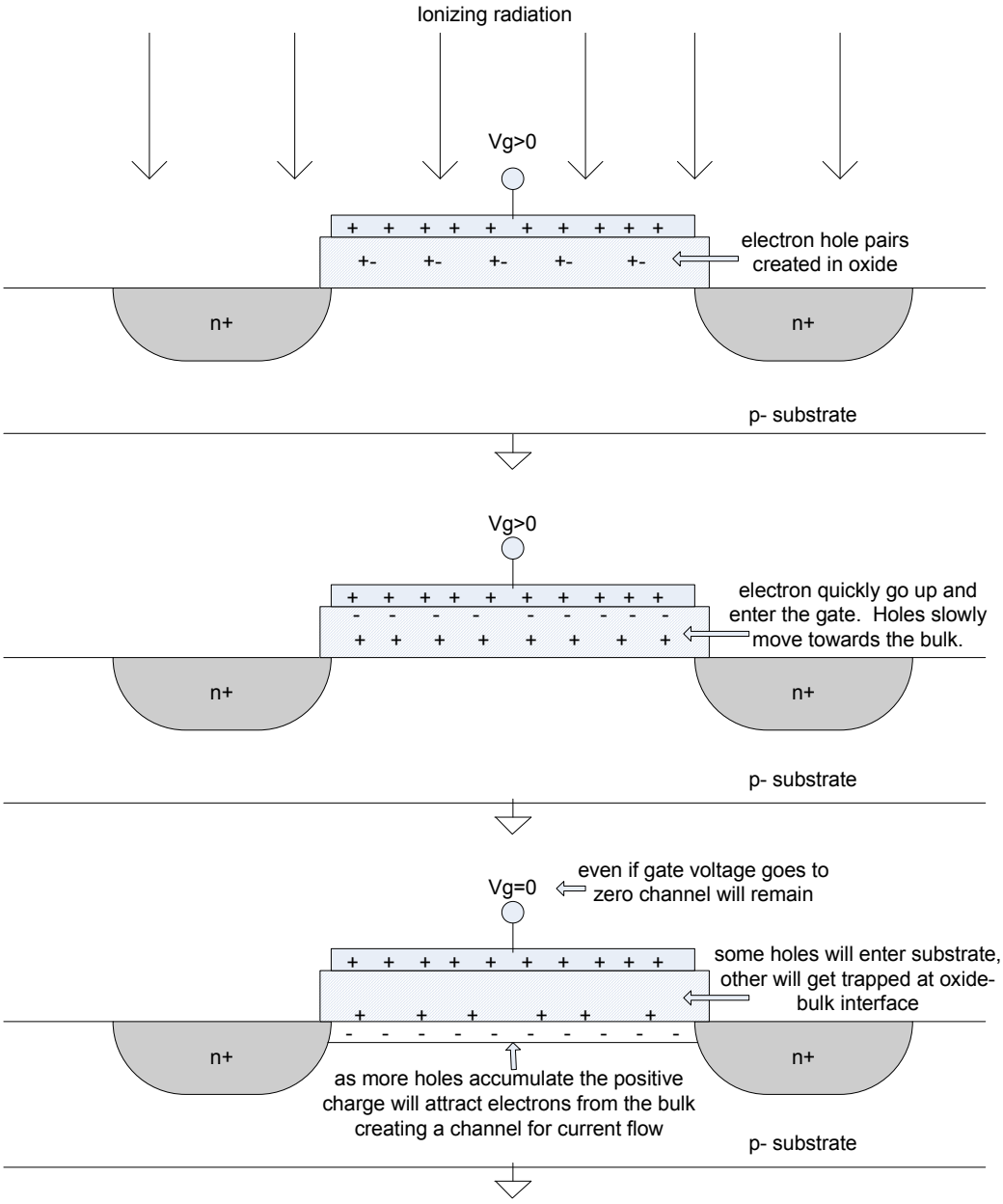

Figure 2.1: Process of Trapped Holes Creating a Bias Independent Channel

a p-channel device should not be biased with a positive voltage with respect to the n-type well, but instead a negative one with respect to the well, so the holes will move towards the gate instead of the well and never become trapped in the oxide-well boundary. The channels formed are present even when there is no applied voltage to the gate of a transistor making it so the device has current flowing between the source and drain even when the device is biased to be turned off. This current can be split into two parts, subthreshold and device currents [7].

The subthreshold current is the current that flows through the channel created between the source and drain, in the same location where the channel would be formed if a gate voltage, above the threshold voltage, were applied. This channel and the subsequent sub-threshold current are present if there are trapped holes in the gate oxide-substrate boundary. The device current is from the channel that can be formed on the edge of the device where the gate comes up over the field oxide in the region known as the bird's-beak region, see Figure 2.2.

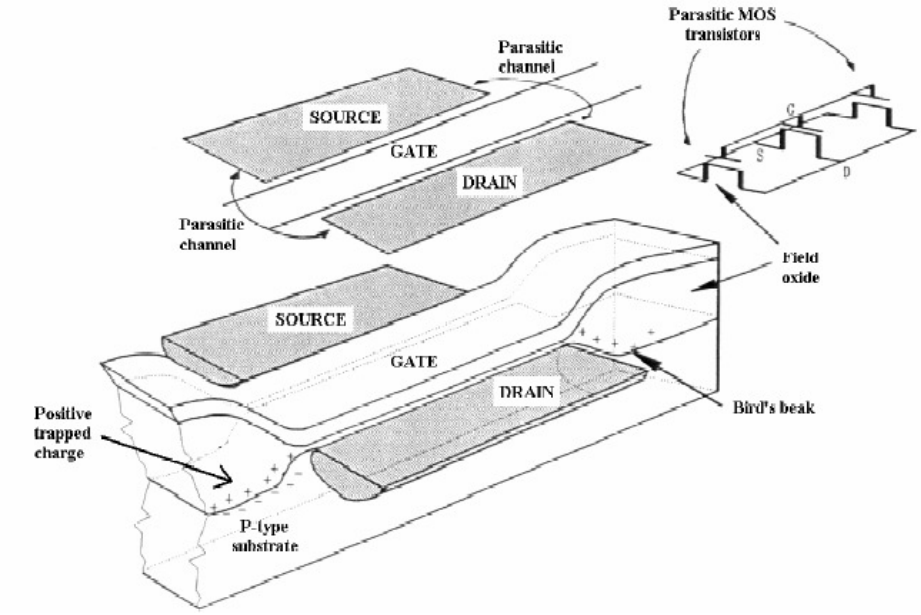

Figure 2.2: Illustration of Bird's Beak Region with Trapped Holes [7]

The trapping of holes in the gate oxide can be greatly reduced to being, for many purposes, insignificant by using a process that has a thin gate oxide that is less than 10nm. Most modern deep sub-micron processes have thin gate oxides that meet this requirement. The remaining problem is then the hole trapping in the bird's-beak region, since field oxide is normally much thicker than the requirement for negligible hole trapping. The effect from device current flowing through the channel formed in this region can be seen, at multiple total-dose levels, for a rectangular gate transistor, in Figure 2.3 for a 0.35um process. Figure 2.4 shows results for an annular FET, a type of FET that is to be

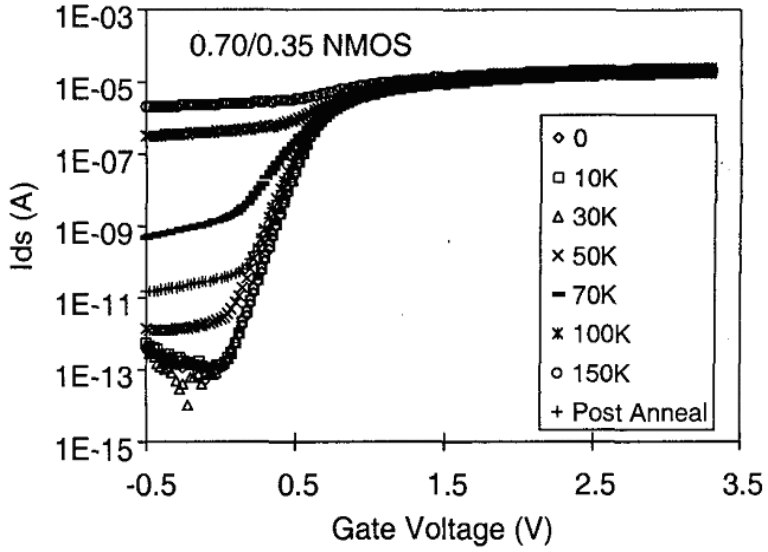

Figure 2.3: I_{ds} vs. V_g for a Rectangular FET at Different Total-Dose Levels [9]

discussed that uses a non-rectangular layout to limit the amount of device current, using the same 0.35um process as the rectangular FET measured for Figure 2.3. The rectangular FET can be seen to only be radiation tolerant to 50krad, while the annular FET is radiation tolerant above 2Mrad. This great increase in radiation tolerance illustrates the motivation that is present to design FETs with non-rectangular gates for the purpose of reducing the device current.

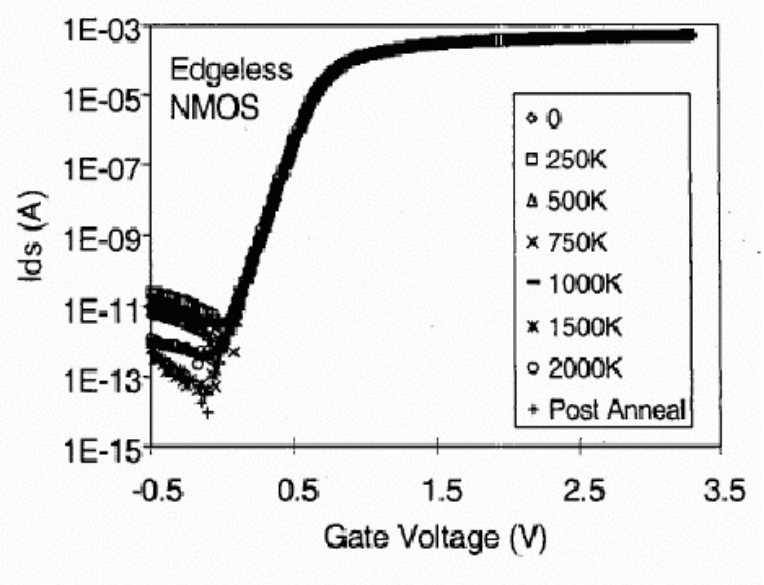

Figure 2.4: I_{ds} vs. V_g for an annular FET at different total-dose levels [9]

SECTION THREE

DESIGN AND LAYOUT OF RAD-HARD FETs

3.1 Annular FETs

Annular FETs have an abnormal gate geometry and have been a highly studied [1],[3],[10],[11],[12]. An example layout of an annular FET can be seen in figure 3.1. The main reason for the study of these devices is that they can provide for more than an

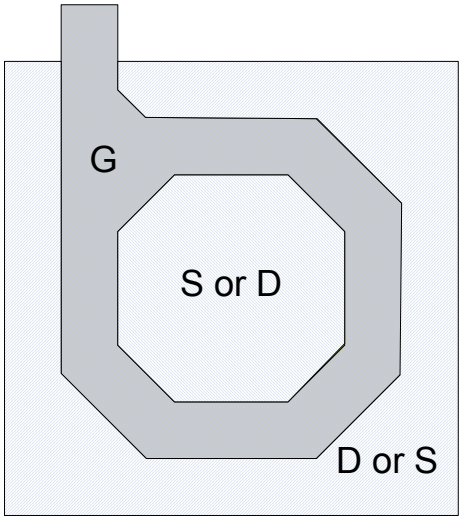

Figure 3.1: A Layout of an Annular FET

order of magnitude improvement in total-dose radiation tolerance, as seen in the last section [9]. The reason for the great improvement in radiation tolerance is that the annular FET has drain or source, but not both, on the two sides of the bird's-beak region. Hence, even if there is a channel formed in that region, there is no potential across it to induce current flow. An annular FET can also be found useful because it has a smaller C_{gd} in the saturation region if the drain is on the inside of the gate than a standard FET of equal W_{eff}, the effective width of the gate, because the inner perimeter is smaller than W_{eff}. Since C_{gd} is often multiplied by the Miller Effect and often is a key component in

the placement of device poles, it can be advantageous to minimize it [13]. This minimization will come at the cost of a decreased output resistance, R_{out}. If the drain is placed on the outside of gate instead, the output resistance will be increased [1],[3]. This increase can help circuit parameters, such as the gain of an opamp design. One last advantage of an annular FET is that the source or drain, which ever is on the inside of the gate, node will get less leakage through the substrate to that node. The reason for this is the outer node and the gate will act as a guard ring protecting the inside. To model this FET it is necessary to find what the effective width and length are, correct for the change in R_{out} and the effect the geometry has on the device capacitances.

3.2 Horseshoe FETs

The horseshoe FET, Figure 3.2(a), is a new FET design, but is similar to a previously proposed design of a Dog Bone FET, Figure 3.2(b) [14],[15]. Both FETs limit

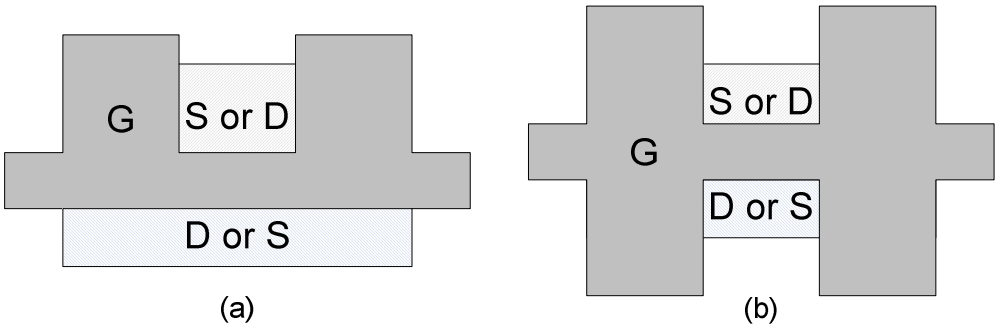

Figure 3.2: A Layout of a Horseshoe FET (a) and a Dog Bone FET (b)

the effect radiation has on the device by lengthening the channel formed under the bird's beak region from source to drain along where the gate comes up over field oxide. As a result the effective (W/L) ratio of that device channel is decreased. This then decreases the amount of device current proportionally. This device requires a higher total-dose level to obtain the same amount of device current as a FET without an increased device channel length. Another advantage is that the minimum achievable (W/L) ratio of the

FET can be arbitrarily small; while it has been shown for annular FETs in a 0.25um process that a minimum (W/L) ratio of around 2 is achievable [3]. Also, the area consumed by a horseshoe FET can be made to be much smaller in area than annular FETs. Design rules can cause the minimum size of an annular FET to being over 2um and 1.5um on a side for a typical 0.25um and 0.18um processes respectively, which can become inhibitive if many rad-hard transistors are needed. To model these types of FETs the width and length will again need to be determined along with asymmetric output resistance and the effect of their geometry on device capacitances.

3.3 Gate Around Source and Gate Around Transistor FETs

Gate around source, GAS, Figure 3.3 (a), and gate around transistor, GAT, Figure 3.3 (b), style FETs employ another method for providing for radiation tolerance. Nodes

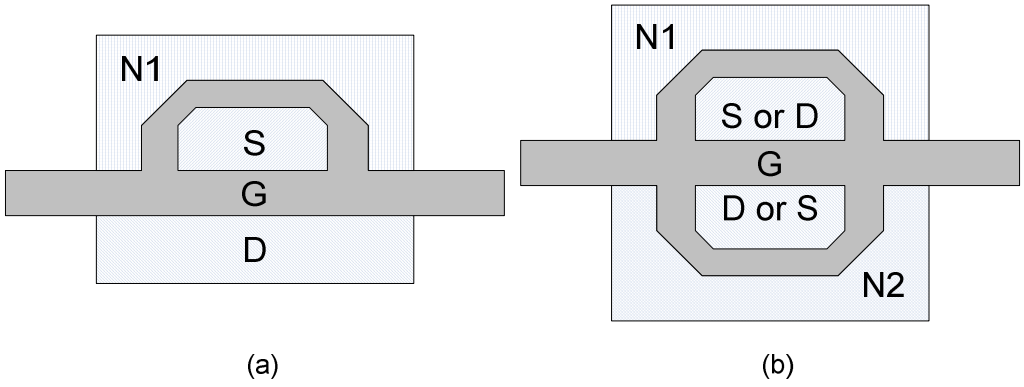

Figure 3.3: A Layout of a GAS (a) and a GAT FET (b)

N1 and N2 are not set to a specific voltage in these layouts, but their voltages can be calculated because the current flowing through the nodes is a set by the gate and source voltages. To understand how these FETs are radiation hardened it is useful to break these complex FETs into simple FETs as in the schematics shown in Figure 3.4 GAS(a) and GAT(b). By observing the layouts it can be seen that for the GAS FET the transistor that is created with a source at the source of the total device and a drain at N1 will not be

affected by device current. The transistor between N1 and the drain will be. Since both the FET between N1 and the source and the FET directly between the source and the drain of the device have no device currents, the current from source to drain will still be able to turn off. The device will still be affected by device current when active and would not be suitable for accurate analog circuits. It can be used for digital applications because it still has an on and an off region. By observing the GAT FET a

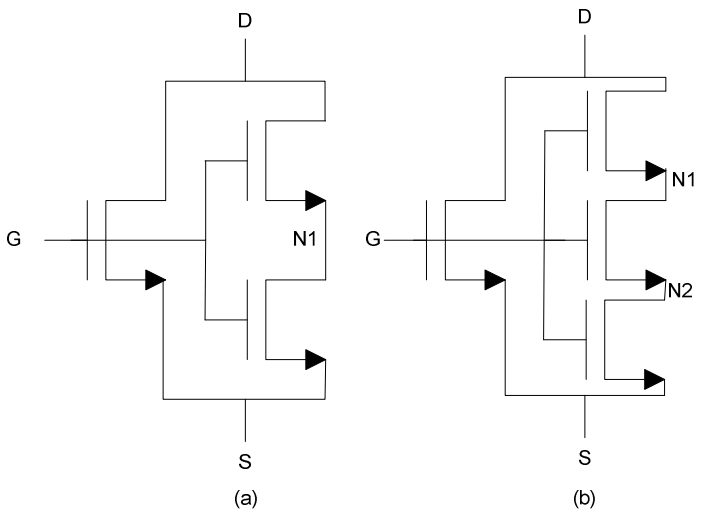

Figure 3.4: A Schematic of a GAS (a) and a GAT FET (b)

similar behavior can be noticed, except this device is symmetric. The source contact and the source and drain contacts for the GAS and GAT FETs respectively are protected by the surrounding gate like an annular FET's inner contact. These devices have no significant advantage over an annular FET, because they are still very large and can be affected by radiation when in saturation.

3.4 Design of a Test Chip

To study the devices mentioned above, test chips were created containing many DC structures with all four FET terminals available for biasing. These structures can be

used for characterization of I_{ds} vs. V_{ds} for different gate voltages, as well as other DC sweeps. This provides verification for the widths, lengths and the R_{out} of the associated models. Also, large probeable RF structures were built to allow direct measurement using a C-V meter of some of the device capacitances of the devices studied. The RF structures may also assist in the development of high frequency small signal models of these devices in the future. Lastly, 13 stage ring oscillators were added with different types of transistors as capacitive loads. The idea was that if the loads were put into different regions of operation, a difference in the frequency of oscillation could be detected giving a relative size of the capacitive load. The ring oscillators were incorrectly laid out when multiple modifications had to be made near the deadline for sending the design to fabrication and they were non-functional. These test chips were designed and fabricated in TSMC 0.25um and 0.18um processes to test the models for scalability and because these are currently commonly used processes. The fabrication was done through MOSIS. These test chips will also be used to test the total-dose tolerance of these devices at theBoeing Radiation Effects Laboratory (BREL) using a Cobalt-60 gamma source at 50 rad(Si)/sec.

3.5 Pi FETs

One other type of FET was included in the test chip. This was a Pi FET, see Figure 3.5. The thought was that this would act like one side of an annular FET. The

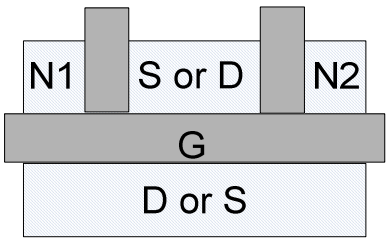

Figure 3.5: A Layout of a Pi FET

goal would then be to get increased output resistance, with a smaller size than an annular FET. It was thought that this layout could be used in low power applications with a higher R_{out} than a rectangular FET. This R_{out} would not be as high as that of a cascode, but would have a higher output swing, which can be advantageous if the supply voltages are small. The device did have an asymmetric output resistance that can be higher than a standard FET, but if the device is split into simple FETs it can be observed to have a cascode in it, just like a GAS or GAT FET, Figure 3.4, so no advantage is gained. Also this FET is not radiation hardened in any way, because the simple FETs that it can be split into all have gates that come up over the bird's beak region at some point. For these reasons this device will not be examined further in this thesis, but it can be analyzed in the same way that this thesis suggests for GAS and GAT FETs.

3.6 Corrected GAS and GAT FET Layouts

If the gate of a GAS FET is extended to the edge of the active region, a new enclosed layout can be created, as seen in Figure 3.6. Similar changes can be made to a

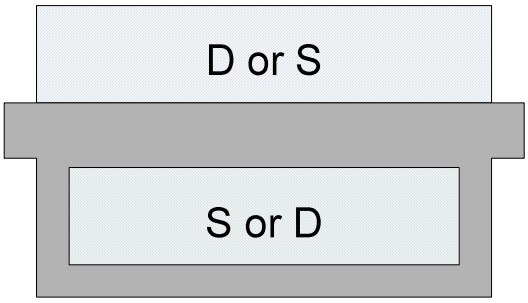

Figure 3.6: Corrected GAS FET Layout

GAT FET. This removes the additional FETs that were unintended in the original layout. One advantage to this layout is that since the source and/or the drain are completely enclosed the total-dose tolerance is similar to an annular FET, but the device can be made to take up less area than a minimum annular FET for typical design rules. Also, if the

gate around the edge is kept at a set length while the gate directly between the source and the drain has it length continuously increased, a smaller (W/L) ratio, than the minimum for a typical annular FET layout style, can be achieved. A corrected GAT FET layout would be typically larger than a minimum annular FET, but a GAT FET has both the drain and the source protected by gate from leakage. To get the same protection, an annular FET would have to have an additional guard ring which would cause the annular FET to become significantly larger than the corrected GAT FET. No corrected GAS or GAT FETs were fabricated, but the methods proposed for annular and horseshoe FETs can be used for this gate geometry as well.

SECTION FOUR

METHOD FOR CREATING MODELS

4.1 Requirements for a Useful Model

To create a model that is useful to circuit designers, a modified SPICE model should be developed based on the SPICE models provided by the foundry of choice, BSIM3 models in our case. Foundries put a large effort into creating accurate SPICE models that characterize process variations and temperature dependencies. Basing abnormal gate geometry FET models on the foundry SPICE models utilizes all of this knowledge. The models should be accurate in all regions of operation. The models should be complete including all significant differences between the behavior of a rectangular gate FET and the chosen FET with an abnormal gate geometry. If this is provided to the designer, the number of redesigns necessary will be reduced and the yield will be increased, because of better matching between simulation and testing. To this end, the models created will be presented along with the necessary changes to a BSIM3 model to make the new model accurate for a given device.

4.2 Groups of FETs to be Studied

The FETs with abnormal gate geometries that are to be studied can be split into two main groups. The first group includes transistors with abnormal gate geometries that 1) limit the amount of device current by lengthening the channel formed to allow this current to flow or 2) by making it such that the bird's-beak region does not have a potential across it such that the region only borders the source or the drain, but not both. Annular, horseshoe and dog bone FETs, seen is section 3, are in this category. The

second group uses additional “dummy” FETs, to shield the effects of radiation from the “main” FET, the FET that is directly between the source and the drain of the total device. The “dummy” FETs do affect the behavior of the total device but, even with large possible amounts of leakage currents into some of the “dummy” FETs the device will still be off in the cut-off region. This group consists of multiple non-parallel transistors that share a common gate with an abnormal geometry. Gate around source, GAS, and gate around transistor, GAT, FETs, seen in section 3, are in this group.

4.3 Modeling of Single FETs with an Abnormal Gate Geometry

The first group can consist of any geometry including annular gates, horseshoe gates etc. The only requirement on the geometry is that there are clear parameters that can be used to uniquely define it, often the corners of a polygon are sufficient for devices that meet design rules for most modern processes. For devices that are in this category, the equivalent width and length have to be found as well as the asymmetric effects on the output resistance and the effects the geometry has on the device capacitances.

Width and Length Determination

The first parameter that is often found for these devices is the aspect ratio or (W/L). Some people have very roughly assumed this to simply be the geometric mean W of a shape, or the mid-line approximation, divided by the common length across a device. The common length is the length that is the shortest distance from the source to the drain, or vice versa. See Figure 4.1 for a better understanding of this and the mid-line approximation. This approximation is, in general, not true and can provide very inaccurate result in many cases [1]. To be more accurate, one method people have turned

towards to find (W/L) is the use of 3D simulation software to extract this for a given geometry [3]. This can be very accurate but very time consuming and complex compared

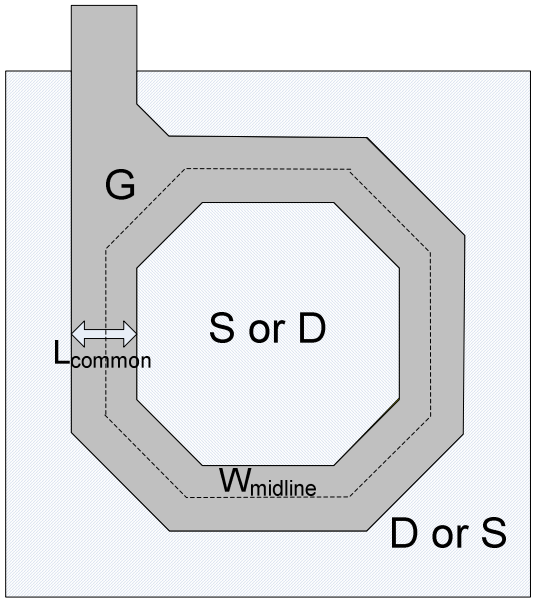

Figure 4.1: Annular FET Layout Showing the Common Length and Midline

to an alternative method that has been applied before to a few geometries, but will be improved upon in this thesis.

The other, often overlooked, method for finding the (W/L) ratio of a FET with an abnormal gate geometry involves conformal mapping [16]. The concept is that a geometry can be mapped onto another according to the Riemann mapping theorem [17]. For circuit designers this is useful because it allows the mapping of a gate with an abnormal geometry to a rectangular geometry which has a well characterized and well understood model. See the conceptual diagram of conformal mapping in Figure 4.2. The rectangle found in the end will have a specific (W/L), or aspect ratio. This aspect ratio can then be used for the drain current equations for the FET.

For some geometries, such as a concentric or eccentric rings, a closed form solution can be found for mapping the given geometry onto a rectangle. For other

geometries, trapezoids, polygons and most shapes that can actually be designed as gates, using typical layout rules, no closed form solution can be found and a more complicated

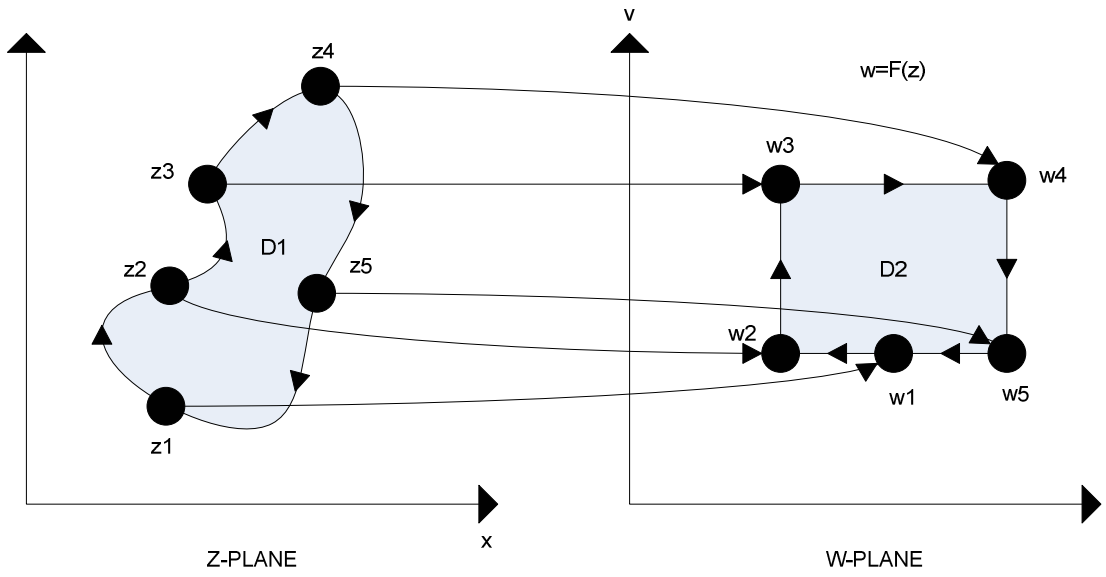

Figure 4.2: Conformal Mapping from an Abnormal Geometry to a Rectangle

method must be used to find the aspect ratio. The more complex method involves the use of the Schwartz-Christoffel transformation in the conformal mapping. The Schwartz-Christoffel transformation involves the use of an intermediate plane to which both geometries can be mapped using the appropriate functions [17]. In the case being considered, one geometry would be an abnormal gate geometry and the other would be a rectangle. So, the abnormal gate geometry can be mapped to the intermediate plane by an appropriate function and then the inverse of the mapping, which would be required to bring a rectangle onto that plane, can be used on the intermediate result to get the desired rectangle. See the conceptual diagram of this in Figure 4.3. The mapping involves complicated integrations that can often only be handled numerically. Software packages exist for mapping a given geometry onto a rectangle. One such package, the one that was

used for this work, is the SC toolbox for Matlab found at:

http://www.math.udel.edu/~driscoll/SC/.

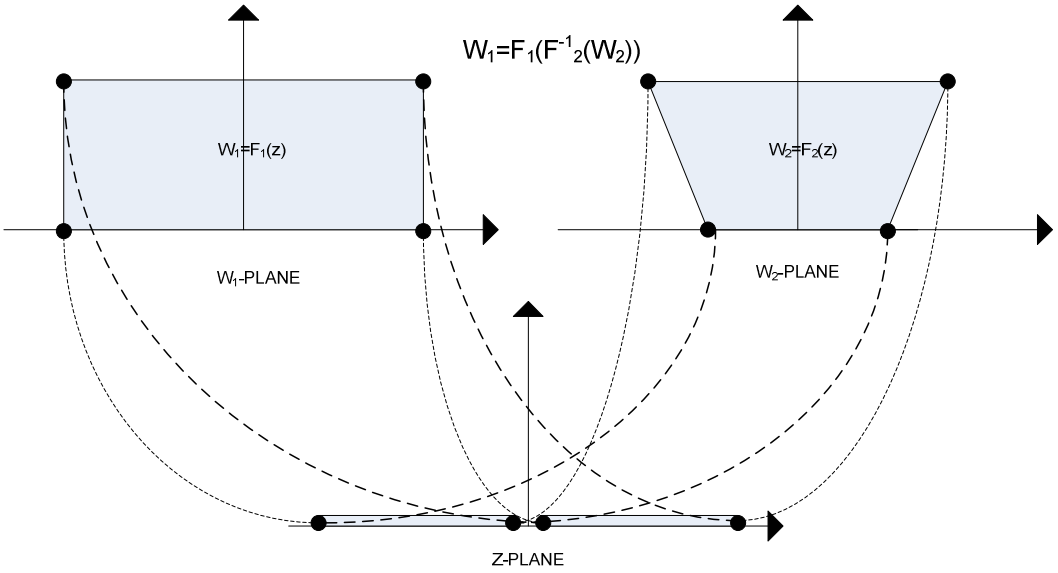

Figure 4.3: Mapping using Schwartz-Christoffel Transformation

For any device the resulting (W/L) found from the conformal mapping will be accurate. But, it is important for modern processes, which exhibit short channel effects, to know the appropriate W and L, not just the ratio of the two. Most importantly, the length, L, can affect the drain current in very noticeable ways, other than affecting just the multiplying ratio (W/L). Because of this, it is necessary to determine the appropriate length and then, using the found aspect ratio, find the correct width.

To find the length that should be used for high accuracy models, it is useful to split this issue into two types of problems. The types are common length problems and complex length problems. The common length problem is a simplification where one notices that nearly all of the current in the channel flows across equal length paths from source to drain. Remember, the common length was defined earlier. This simplification will not be completely accurate for any gate geometry except rectangular ones but it can

be employed in some cases and still be reasonably accurate. The second group is any device where the geometry is such that the paths the current takes vary noticeably in length and an accurate solution can not be obtained using the simplification. The method presented for the complex length problem, if used correctly, can give more accurate results for any geometry, but may not be necessary in some cases. Previously, people have treated all geometries like a common length problem, but as will be seen in section 5, this can cause significant errors [1],[3]. A way to visualize the different path lengths is to plot a rectmap object with the SC toolbox. This will plot equal-potential lines from the resulting rectangle mapping to the corresponding lines on the abnormal gate geometry, see Figure 4.4. To decide which type of problem approach should be used, one can calculate the average of several of these equal-potential lines. If the average is close to

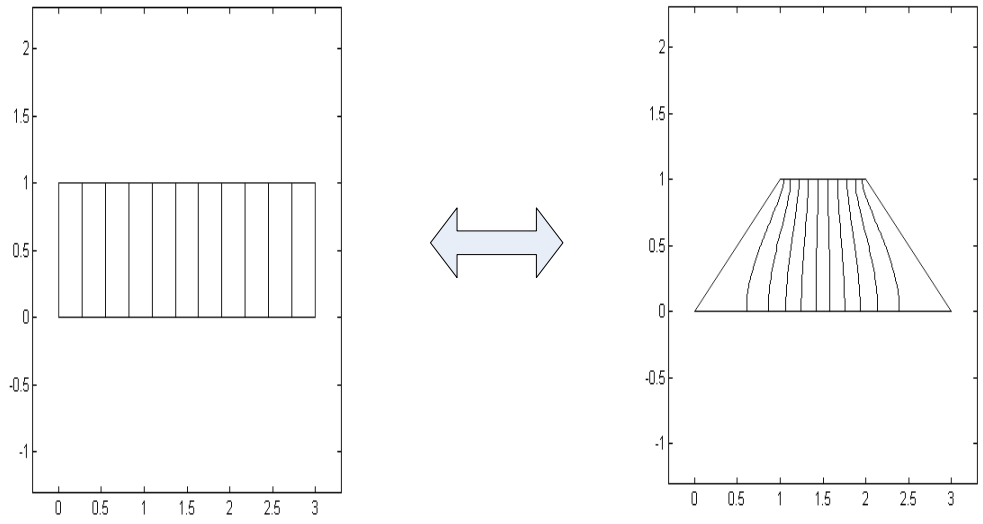

Figure 4.4: Mapping of Equal-Potential Lines

the common length, the common length can be used. Otherwise, the problem should be addressed as a complex length problem.

The complex length problem does not just use the common length or a calculated

average of path lengths as both can be found to have large errors, as section 5 shows. Instead, multiple equal-potential line lengths should be found on the abnormal gate geometry and then that many transistors should be placed in parallel to obtain the model. Each transistor will represent the region between an equal-potential line and the next. The more line length calculations that are used for the model, the more accurate the end results will be. This can be seen in section 5. The width of each parallel transistor, before any are combined, is then the found aspect ratio of the rectangle, $\left(W/L\right)_{rect}$, divided by the number of parallel transistors and then multiplied by the length of the region, L_{region}, or:

$$W_{region} = \left(W/L\right)_{rect} * L_{region} / (\text{number of transistors}) \qquad (4.1).$$

This preserves the aspect ratio of the region of the rectangular gate, which the given geometry has been mapped to, that the individual transistor represents. If multiple transistors with equal, or close to equal, lengths are combined, the width of the combined transistor is just the sum of the individual widths and the length is the common length. To find the average length and the length of the individual, lines replace the function rplot, included in the SC toolbox, with the one provided in the appendix of this thesis and then run the plot function on a rectmap object. An important note is to use the SPICE model that has been described to be accurate for the length being used for that region and the total width of the device, not just the region's width even though the W_{region} becomes very small as more regions are used. The reason for this is that if the model for the smallest width devices is used, narrow channel effects will cause errors because the total channel is not narrow.

Asymmetric Output Resistance

The next effect of geometry that should be taken into account for this type of FET is the non-symmetric behavior in the saturation region. This is due to the effect of channel length modulation being different depending on what side of the transistor is being used as the drain and how this compares to a standard rectangle [1],[3]. The reason for this difference has previously been described and has to do with conservation of space-charge. If a rectangle of a certain width is mapped onto another shape, space-charge must be conserved in the region affected by channel length modulation. If a region is mapped onto another region that is wider, for example, the ΔL, caused by channel length modulation, would be smaller on the wider region such that $\Delta L * W_{region}$ is constant. The opposite would be true if a region is mapped onto a narrower region. See Figure 4.5 for a visual representation. The geometry's effect on Rout can be found from

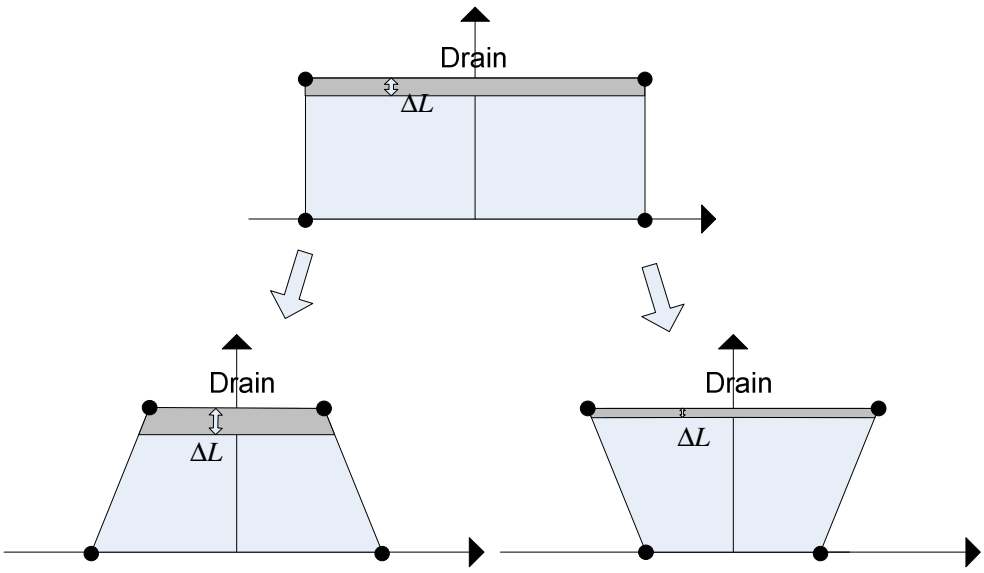

Figure 4.5: Space-Charge Conservation in the Channel Length Modulation Region Across a Mapping

the new ΔL found for the region of the abnormal gate compared to what it would be for that region mapped onto a rectangular gate. Rout can be expressed by the equation:

$$R_{out} = \frac{\Delta V_{ds}}{\Delta I_{ds}} \cdot \frac{L_{region} - \Delta L}{\Delta L} \quad (4.2).$$

Next, the percent difference between two R_{out} values, one for a rectangular region and the other for a abnormal region can be define as:

$$\Delta = (R_{out\_rec} - R_{out\_ab}) / R_{out\_rect} \quad (4.3).$$

By using equation (4.2), we find that:

$$R_{out\_rec} = \frac{\Delta V_{ds}}{\Delta I_{ds}} \cdot \frac{L_{region} - \Delta L_{rec}}{\Delta L_{rec}} \quad (4.4)$$

and

$$R_{out\_ab} = \frac{\Delta V_{ds}}{\Delta I_{ds}} \cdot \frac{L_{region} - \Delta L_{ab}}{\Delta L_{ab}} \quad (4.5).$$

Where ΔL_{rec} and ΔL_{ab} are the effect of channel length modulation on the rectangular region and the abnormal region being compared respectively. If then (4.4) and (4.5) are substituted into (4.3) and use of the fact that $\Delta L * W$ is constant a new equation can obtained:

$$\Delta = 1 - \frac{W_{ab}}{W_{rect}} \cdot \frac{L - \frac{W_{rect}}{W_{ab}} \cdot \Delta L_{rect}}{L - \Delta L_{rect}} \quad (4.6).$$

The length being used is either the common length or the length of an individual region found with the complex length method. Also, ΔL can be approximated as the amount the length would have to change to make the ideal FET I_{ds} vs. V_{ds} curve deviate by enough to have the same current as a simulated FET, without output resistance correction, at a

point on the curve in saturation. See Figure 4.6 to understand this better. As the drain voltage increases, the effective length decreases and the ideal curve in saturation shifts upwards on the graph. So, at different points, the amount the length has changed by can be found by comparing the ideal plot with the simulated one for a standard FET of the

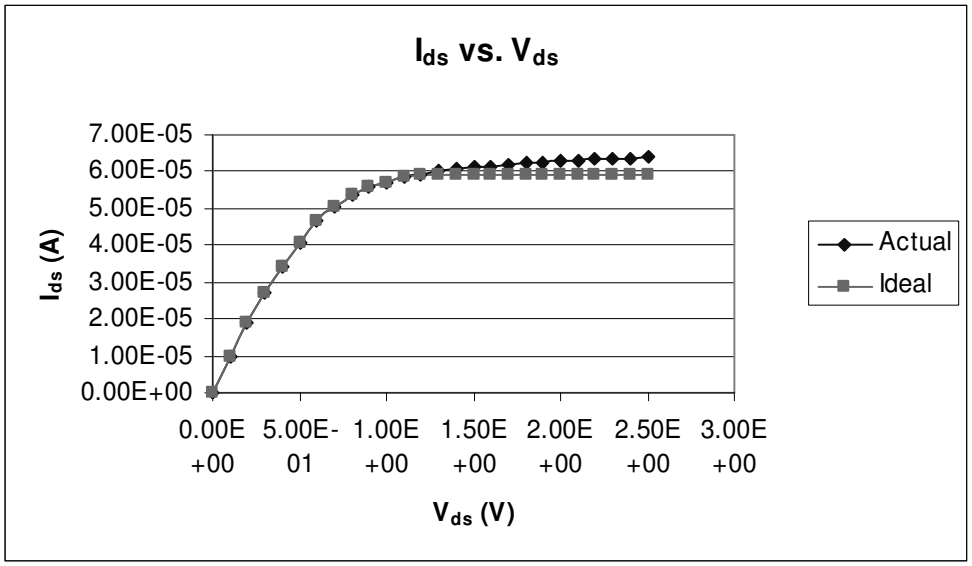

Figure 4.6: Ideal vs. Actual curves for I_{ds} vs. V_{ds}

given width and length. The resulting ΔL is roughly:

$$\Delta L \cong L \cdot \left(1 - \frac{I_{ds\_actual}}{I_{ds\_ideal}}\right) \tag{4.7}.$$

Equation (4.5) assumes the current will change linearly for a small length change. The R_{out_ab} at that point should be:

$$R_{out\_ab} = \frac{R_{out\_rect}}{1-\Delta} \tag{4.8}.$$

This method was used previously [3], but without multiple regions. The ratio of the distance along the gate that bordered which ever side of the device was called the drain to the width that was found using the aspect ratio along with common length in the

calculation for Δ was used. This is over simplified because it assumes the equal-potential lines are evenly spaced on the new device along the drain, but with a larger or smaller spacing than for the rectangular device the geometry can be mapped to. This is not true for most devices and, instead, the equal-potential lines will not be evenly spread as was seen earlier in Figure 4.4. The simplification has been found to often have 20%-40% error in Rout from measurements for an annular FET [3].

A more accurate approach is to use the ratio of the distance along each region that borders the side that is being used as the drain to the width given by (4.1). By splitting this into parts and taking the ratio region by region, a more accurate Rout can be obtained because this takes into account the non-even spacing of the equal-potential lines and the fact that ΔL will not be constant along the drain. Figure 4.7 shows a comparison of the previous approximation to the new more accurate one and an estimation of what the actual profile of ΔL would be for an example shape. As with the calculation for the lengths, the more regions that are used to get the effect the geometry has on R_{out}, the more accurate the solution will be.

To then change the BSIM model to have the correct Rout, the parameter PCLM can be changed. PCLM is one of the main parameters that affect how channel length modulation affects the device's behavior. Changing this parameter is reasonable because it is the channel length modulation that is not the same compared to the rectangular device. A search algorithm was used to obtain a value that had good matching to the result from (4.6) at a point or to minimize the error over many points in saturation. This must be done for each parallel transistor that makes up the total model. This means that

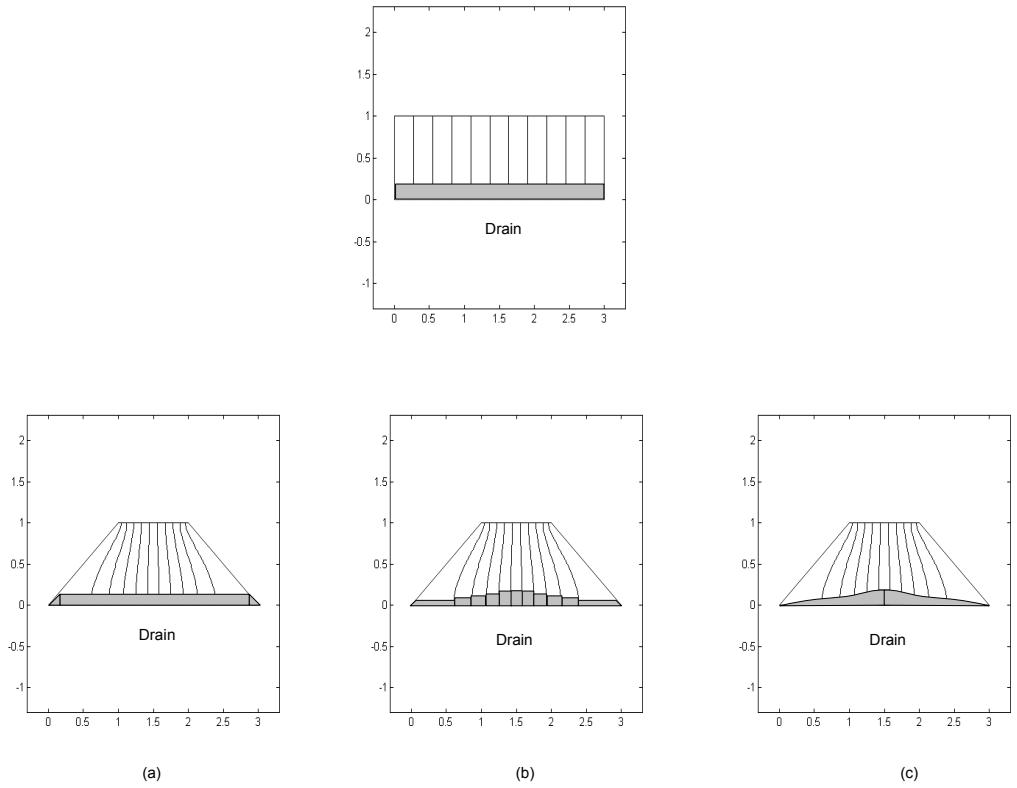

Figure 4.7: Space-Charge Conservation from a Rectangle to a Trapezoid Using (a) the Previous Approximation, (b) the New Approximation Used in this Thesis and (c) an Estimation of the Actual Channel Length Modulation Profile.

each transistor will have to have a separate model or the model must be in a version of spice where a parameter can be passed to the FET model for the different PCLM values found. If fitting would require PCLM to become a negative value, which is not allowed by SPICE, then the length, L, can be changed to get the correct output resistance and the width, W, can be changed to again have the correct current in non-saturation. At this point, if faster SPICE simulations are desired, the parallel FETs, using the corrected W, L and PCLM parameters can be simulated and then a single FET model can be fit to the device. This fitting to a single device was not performed on the results presented in this

thesis, but with IC-CAP or a similar fitting tool a single SPICE model can be developed to match the parallel FETs to within about a percent.

Device Capacitances

The last significant difference compared to a rectangular FET that needs to be taken into account to model this type of FET is the affect the abnormal geometry of the gate has on the device capacitances used in a typical small-signal model shown in Figure 4.8 [18]. The capacitances shown in the model and the affect the geometry has on their values will be discussed. It is good to note that this model is for low frequencies. RF measurements and models have not been performed. A previous way to model the

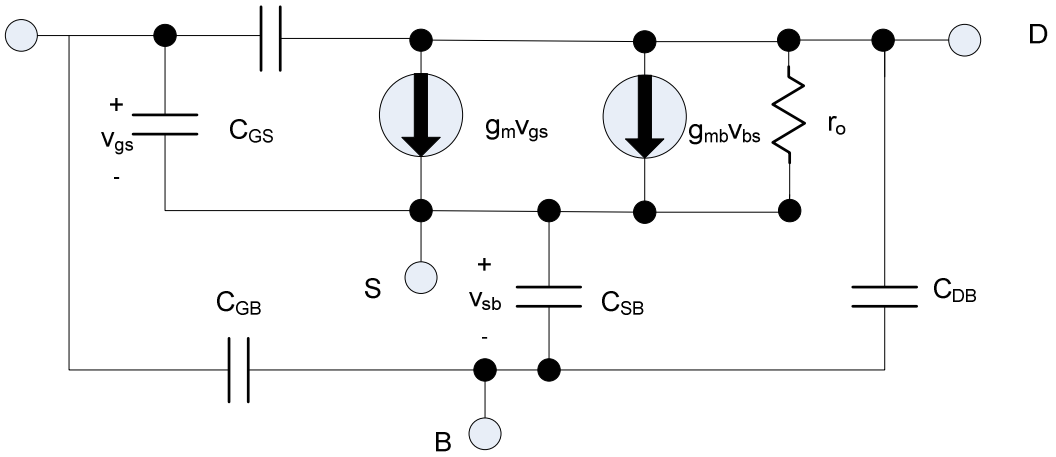

Figure 4.8: Small-Signal FET Model

capacitances of an annular FET has been published, but was incorrect [1].

For the intrinsic capacitance to be modeled correctly in SPICE a few parameters need to be modified. The standard FET model assumes the area of the gate to be

$$Area_{gate} = W_{active} * L_{active} \tag{4.9}$$

where

$$W_{active} = W - 2*DWC - (other\ terms) \tag{4.10}$$

and

$$L_{active} = L - 2*DLC - (\text{other terms}) \quad (4.11).$$

DWC and DWL are BSIM modeling parameters [19]. Changing these parameters only has an effect on the C-V modeling of SPICE. To get the correct area to be used by SPICE simply choose a W_{active} and an L_{active} such that the equation for $Area_{gate}$, (4.9), is the correct value and then make new values of DWC and DWL that satisfy

$$DWC_{new} = (W - W_{active})/2 \quad (4.12)$$

and

$$DLC_{new} = (L - L_{active})/2 \quad (4.13).$$

DLC and DWC may have values already, but their values are normally very small, so replacing them should not cause large errors, often < 1%. The factors of 2/3 and 1/2 that are multiplied by the area to find Cgs in saturation and both C_{gs} and C_{gd} in non-saturation respectively are not geometry dependant and do not have to be changed [20]. With the changes given, the intrinsic capacitor will be corrected to represent the geometry used. The extrinsic capacitors including the overlap and junction capacitances have to be modified as well.

The SPICE gate to source and gate to drain overlap capacitance parameters, CGSO and CGDO respectively, simply need to be changed to take into account that the distance along the source or drain that borders the gate may be different than the W_{active} set by correcting the intrinsic capacitances. Let W_s and W_d indicate the distance along the source and the drain respectively that border the gate. Then a new CGSO value can be found as:

$$CGSO_{new}=CGSO*Ws/W_{active} \quad (4.14).$$

Similarly, a new CGDO value can be found as

$$CGDO_{new}=CGDO*Wd/W_{active} \quad (4.15).$$

To get the correct gate to bulk overlap capacitance parameter, CGBO, it should be noticed that the length at the point where it comes over field oxide may not be the length, L_{active}, set by correcting the intrinsic capacitances. Also, the gate may not come over the field oxide on two sides as a standard rectangular FET would. The new GGBO value should then be

$$CGBO_{new}=CGBO*L_o/(2*L_{active}) \quad (4.16)$$

where L_o is the total length along the outside of the gate that comes over field oxide. Next, the junction capacitor parameters in SPICE do not have to be changed. Simply send the appropriate inputs PS, PD, AS and AD to the SPICE model such that the parameters actual represent the perimeters and the areas of the source and drain. Changing the parameters as described will correct all the extrinsic capacitance sources. The changes described for the intrinsic and extrinsic capacitances described will make the capacitance values used by SPICE to be correct to what the device will actually have. With the use of the changes in W, L, Rout and the capacitances, designers now have the most complete model for FETs with abnormal gate geometry.

4.4 Modeling of FETs that use "Dummy" FETs

To model these FETs one must first divide the device into individual transistors that are physically present. For a GAS or GAT FET, this can be illustrated by the layouts in Figure 3.3 and the corresponding schematics shown in Figure 3.4. The width and the length of each of the transistors must then be found. If the gate that separates the source and the drain for any transistor is rectangular then the width and length are simply the

drawn width and length. If instead the gate is of an abnormal geometry, the method for finding W and L presented in section 4.3 must be employed. For the GAS and GAT FETs there are regions that are similar to half of an annular FET. If the gate is of an abnormal geometry, Rout will also have to be modified for that transistor as is also described in section 4.3. Once the widths and length have been found the transistor must be put into a sub-circuit as was shown in the schematics in Figure 3.4 and the total device can be modeled for DC simulations.

To get the correct capacitances for the small-signal model, simply make sure not to double count drains or sources since some are shared. For all transistors that make up the total device for a GAT or GAS FET, the overlap capacitances and intrinsic capacitances, should be treated as normal if the individual transistor has a rectangular gate and as discussed in section 4.3 if the transistor has an abnormal gate geometry. For the junction capacitances, though, changes need to be made. Since some of the FETs share the same physical region as their source or drain, then if the AS, AD, PS and PD parameters are set as normal, then the region will be double counted as junction capacitances. One simple way to fix this is, if two FET share a physical region for source or drain, is set one FET to have the correct area and perimeter for that region and assign the other a perimeter and area of 0 for that region or to attribute half of the area and perimeter to one and the rest to the other. For example, in a GAS FET two of the transistors share the source of the total device as their sources. To not double count the region, set one FET to have AS and PS equal to zero and the other FET with the correct AS and PS from the device layout. This type of FET can be accurately modeled using the

above procedure. As mentioned previously, the same method that is described for a GAS or GAT FET can be used for a Pi FET.

SECTION FIVE

SIMULATION RESULTS USING NEW MODELS AND COMPARISONS TO EXPERIMENTAL DATA

5.1 Method for Acquiring and Simulating Models for Single FETs with an Abnormal Gate Geometry

To generate the DC simulation results for annular FETs or any FET with an abnormal gate geometry Matlab scripts were used. The top level code followed the rest of the code can be found is in the appendix. These Matlab scripts implement the procedures described in section 4.3 for finding the width and length of the parallel transistors to be simulated and the modified output resistance of each of the parallel transistors. The script needs only the argument p set to define the corners of a polygon defined in order, clockwise or counterclockwise, around the geometry. The scripts included show the p vector defining the corners of the first annular FET that will have its simulation results compared to experimental results. The script then uses the Schwartz-Christoffel transformation to find the unique aspect ratio of the rectangle that the geometry given by p can be mapped onto. Next, equal-potential lines are inverse mapped onto the given geometry from the rectangle. The length of each line is initially used as the length of a parallel transistor that will be used later to model the total device. The widths are initially set by equation 4.1.

Next, the spacing between equal-potential lines is found for both sides of the device and this is compared to the equal spacing they would have on a rectangular FET. This comparison results in a ratio of widths that will later be used in equation 4.4. ΔL

for that equation is found by Matlab calling WinSpice and giving it an input file that contains a FET of the appropriate width and length. The results from the SPICE simulation are read in by Matlab and the behavior in saturation is compared to what it would be if the I_{ds} vs. V_{ds} curves had a slope of 0 in saturation. This current ratio between the actual behavior and the ideal behavior then gives an estimate of what ΔL should be, using equation 4.5. With ΔL, a solution to equation 4.4 can now be found, which then allows the solution to equation 4.6 to be found.

To then modify the R_{out} of the device two routines are used. If R_{out} should be reduced by a certain percentage, PCLM is iteratively modified using the secant method to a value that is larger than its original value until SPICE simulations show R_{out} has close to the desired change in R_{out}. If R_{out} should be increased by a certain percentage, PCLM would ideally be reduced, but it would often have to become negative to get the corrected R_{out} that is desired. Instead, the length is changed, to an increased value, along with changing the width using a secant iteration operating on the length with a nested secant iteration operation on the width until the R_{out} is as desired and the I_{ds} values are correct in non-saturation.

In the end the individual FETs are simulated and the results are weighted and summed together for the final I_{ds} vs. V_{ds} curves. The curves are put into three vectors, one for if no R_{out} modification is used, one for if the drain is on the side that will result in higher R_{out}, and one for if it was on the side with lower R_{out}. This process was automated to increase speed and to reduce errors due to manual calculations, which can become quite tedious. A model can be generated in less than 5 minutes on a 1 GHz PC. After the

dc behavior has been corrected, modifications to the capacitance parameters, as described in section 4 should be performed.

5.2 Annular FET Verification

Using the code and process described in section 5.1 and 4.3, simulation results compared favorably to measurements for multiple annular FETs in 0.25um and 0.18um processes. The annular FET defined by the p vector found in the appendix was fabricated in the 0.25um TSMC process. The attached code doesn't have the ability map a completely enclosed geometry, so the annular FET was described as the shape shown in Figure 5.1. Previous work involving 3-D simulations has shown that the other corner of the annular FET on has a slight affect on the total behavior because of the geometry in that region, so it has been excluded [3]. Experimental data was obtained by using a HP4145 controlled over GPIB using Agilent VEE software. The results from simulating

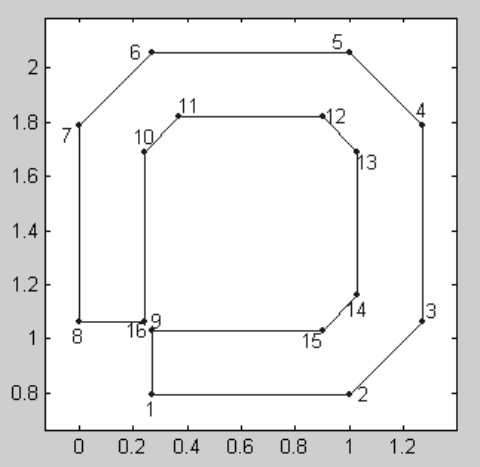

Figure 5.1: Annular FET Entered into Code

the generated model, using 10 parallel FETS, are compared with the experimental data for this annular FET for when the drain is inside the gate and for when the gate is on the outside of the gate in Figures 5.2 and 5.3 respectively. The results show very good matching. The maximum percentage difference between the simulated I_{ds} for any V_{ds}

value for the given gate voltage, 1.5V, and the experimental results was -4.41% if the drain was on the inside and -9.86% if the drain was on the outside. For R_{out}, the

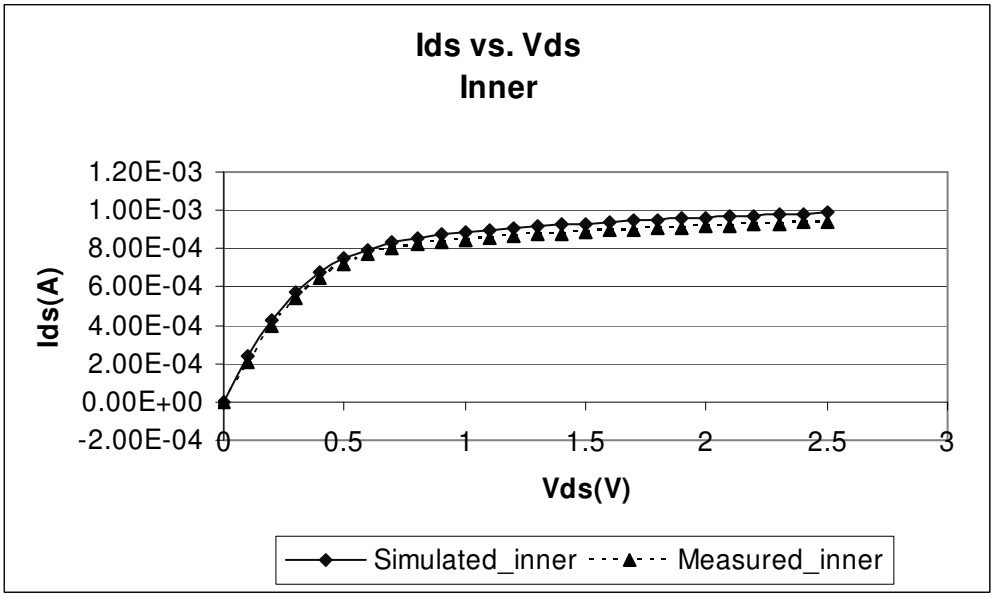

Figure 5.2: Annular FET I_{ds} vs. V_{ds} with the Drain Inside the Gate

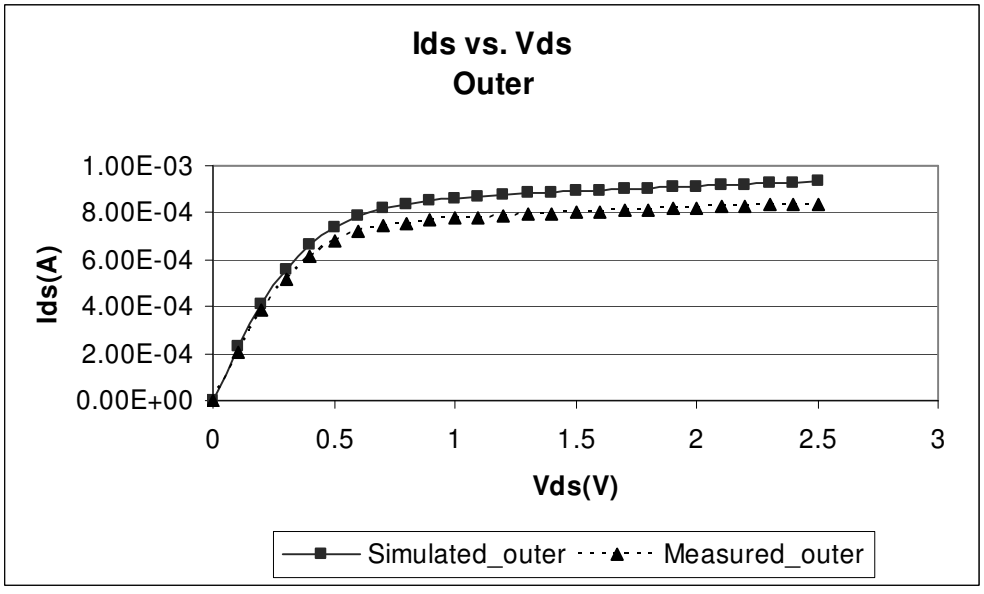

Figure 5.3: Annular FET I_{ds} vs. V_{ds} with the Drain Outside the Gate

difference in saturation was -1.46% with the drain on the inside and 4.75% with the drain on the outside. The R_{out} is the inverse of the slope of the plot. The measurements were only taken on one die and the results are highly accurate and within the possible variation wafer to wafer of the processes used. Measurements for a standard device of minimum gate length showed a 6% higher current in saturation.

The accuracy in non-saturation, without R_{out} correction, was compared to two simulations using the common length estimate, with the common length as the minimum length, 0.24um, and as the average length of the different equal-potential lines mapped, 0.2421um. The I_{ds} vs. V_{ds} curves for these two common length approximations, using 10 parallel transistors along with the accurate model, but now without R_{out} correction, and the actual data is shown in Figure 5.4. As can be seen, all models are almost identical

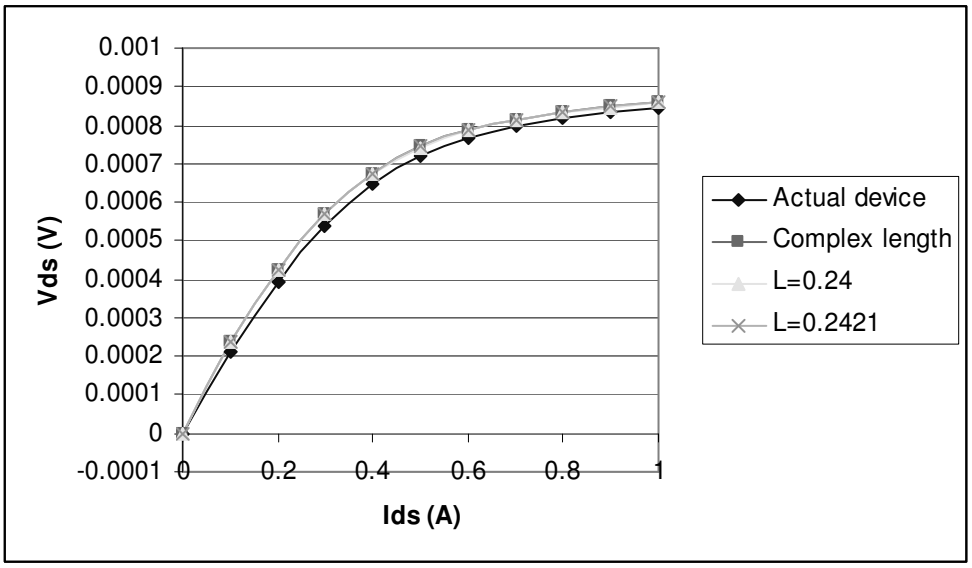

Figure 5.4: Annular FET I_{ds} vs. V_{ds} with the Drain Outside the Gate and Simulation Curves

showing that for this device the common length approximation is a good approximation for drain current magnitude. If the common length approximation is used without

splitting the device into regions for R_{out} correction, large errors result in R_{out}. Then only the simplified approximation using the total ratio of the inner perimeter or the outer perimeter to the width of the rectangular device that has a common length is used in equation 4.4. If the R_{out} is just modified by this factor the errors in R_{out} would be 8.4% for the drain on the outside and 8.1% for the drain on the inside. The error found in this example is about twice the error from using 10 parallel FETs for the drain on the outside and more than four times the error for when the drain is on the inside of the FET. Other annular FETs using the common length method for modifying Rout have had errors, as described in another publications, as high as 20%-40% [3]. This shows that even for an annular FET, a device that has a relatively common length, the new method for modeling provides far better accuracy.

Other annular FETs were simulated in 0.25um and 0.18um process. The maximum error in I_{ds} and the error in R_{out} is listed for each annular FET in Table 5.1 along with their common gate length and the aspect ratio. As can be seen from the table,

Process	L_{common}	Aspect Ratio	R_{out} % error drain inner	R_{out} % error drain outer	I_{ds} max error drain inner	I_{ds} max error drain outer
0.25	0.24	13.896	-1.46	4.75	-4.41	-9.86
0.25	0.24	32.562	-2.35	3.96	-5.13	-8.77
0.25	1	20.5205	-10.7	-4.54	-4.11	-6.88
0.25	1	30.3205	-10.9	-4.48	-5.62	-5.70
0.18	0.18	16.7345	-9.29	1.93	2.64	4.12
0.18	0.18	36.0556	-8.43	-0.52	3.80	2.42
0.18	1	20.5205	-8.02	2.55	3.82	4.45
0.18	1	30.3205	-9.15	6.76	5.09	5.89

Table 5.1: Errors for different annular FETs

the percent error in absolute current was always less than 10% and the percent error in R_{out} was always less than 11% in magnitude. This is very good compared to previous results from other methods. Modifying the SPICE model to better fit the standard FET

for this particular die would presumably further reduce the errors. For example, a standard FET on the same wafer as the other FETs tested for the 0.25um process, with a rectangular gate of length 0.25um, was measured experimentally and it had an output resistance that was 2% higher than the nominal SPICE model and a drain current that had a maximum error of -6%. If this is taken into account for the FETs with a 0.25um length in the same process, the maximum errors in output resistance and drain current are both below 3%. A similar improvement was seen in the results for the FETs in the 0.18um process, when correcting for the errors in the experimental results for a standard FET. Also, the output resistance seems to have a systematic error in the method. If the output resistance for the drain outer configuration is used as a reference, the error for drain inner is always negative with respect to that. Future work could be done to verify this.

For capacitance verification only overlap capacitances and the gate to drain could be directly measured using the test structures available. The measurements were taken with drain as inside the gate and drain outside the gate. The test setup can be seen in Figure 5.5. The modifications that were suggested in section 4.3 can be used to predict what the intrinsic and extrinsic capacitance values should be. Values for gate to drain overlap capacitances and the gate to drain intrinsic capacitances were estimated for the different test structures. First, the gate to drain capacitance was measured in subthreshold, which gives the overlap capacitance which should be the perimeter multiplied by CGDO. Then the capacitance was measured in non-saturation. After subtracting the overlap capacitance would the remaining value should be $0.5*Area_{gate}*C_{ox}$. The corner of the annular FETs cannot be neglected as it was for the DC model, as in Figure 5.1. Because the area has a channel under it in non-saturation and saturation and because it is

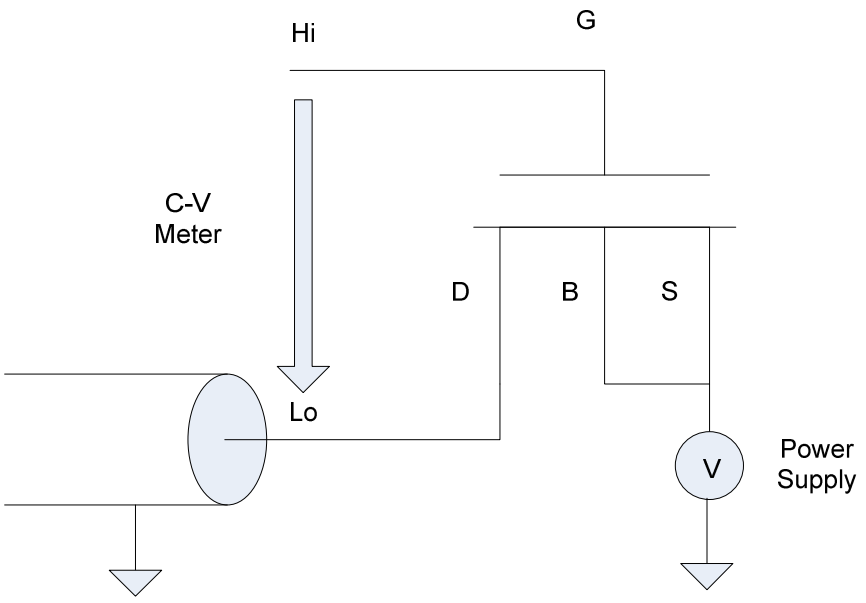

Figure 5.5: Capacitance Measurement Test Setup

physically the same gate it will contribute to both the overlap and the intrinsic capacitances. Matching between the extracted perimeter and $Area_{gate}$ from the capacitance measurements matched to better than 8% for all test structures in both processes. To get this high of accuracy open test structures were used to calibrate out the capacitance of the pads and the interconnect lines.

5.3 Horseshoe FET Verification

For a horseshoe FET the same program is used, but just with a different polygon defining the geometry. Half of the shape was define because it is symmetric about its midpoint, so the results need to be multiplied by two. Because the horseshoe FET's shape shown in Figure 3.2 does not have an obvious common length, the simple common length approximation will be less accurate than with an annular FET. The device is defined to have drain inner if the drain is on the contact that is enclosed on three sides by the gate and drain outer otherwise. Figure 5.6 shows the measured data for drain outer. Poor matching is obtained using the average length or the minimum length in the

common length approximation. The Figure also shows results using 2, 5 and 10 parallel FETs showing increased accuracy as the number of FETs increases. These are without output resistance correction. The next Figures 5.7 and 5.8 show measurements and simulated results with output resistance correction and with 10 parallel FETs, for drain outer and drain inner respectively. Very good agreement was obtained. The maximum percent error between the simulated I_{ds} for any V_{ds} value for the given gate voltage, 1.5V, and the experimental results was -3.84% if the drain was on the inside and -4.91% if the drain was on the outside. For R_{out}, the percent error in saturation was -7.85% with the drain on the inside and 3.54% with the drain on the outside. A similar device was fabricated in 0.18um technology which also had less than 10% error in I_{ds} and

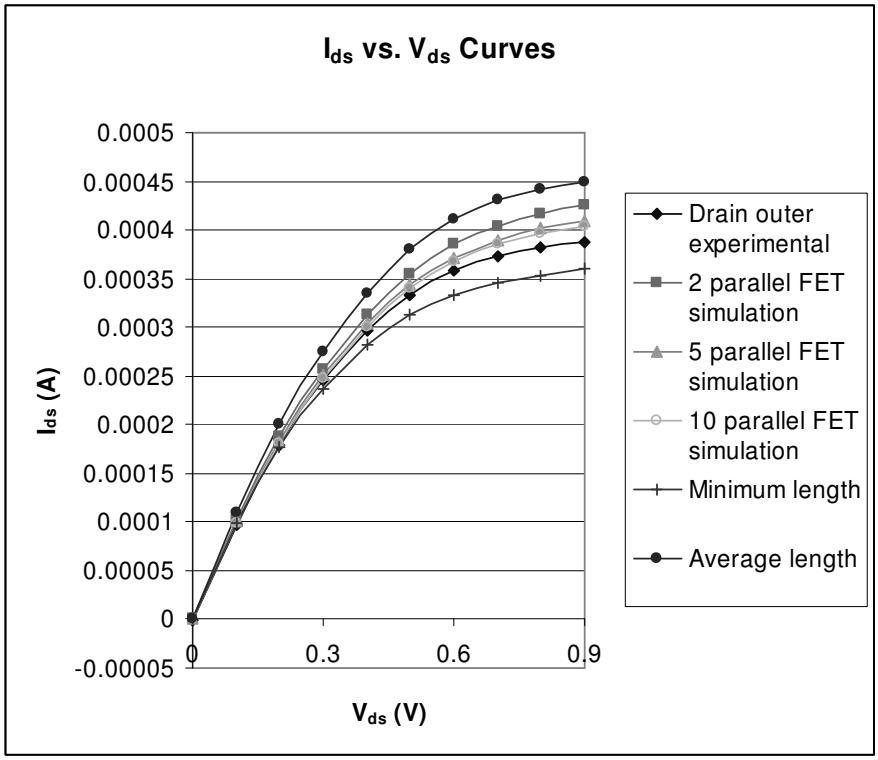

Figure 5.6: I_{ds} vs. V_{ds} with the Drain Outside the Gate and Simulation Curves in Non-Saturation

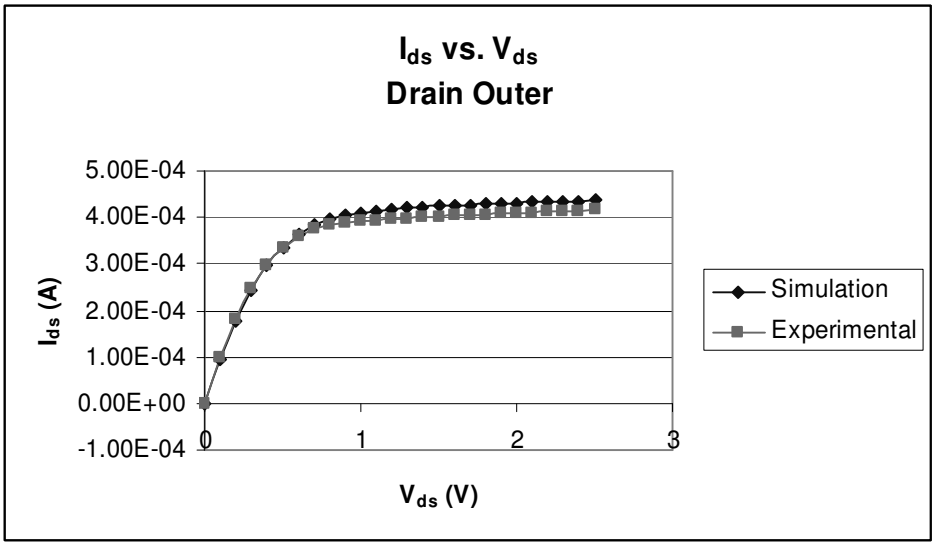

Figure 5.7: I_{ds} vs. V_{ds} for Horseshoe FET with Drain Outer

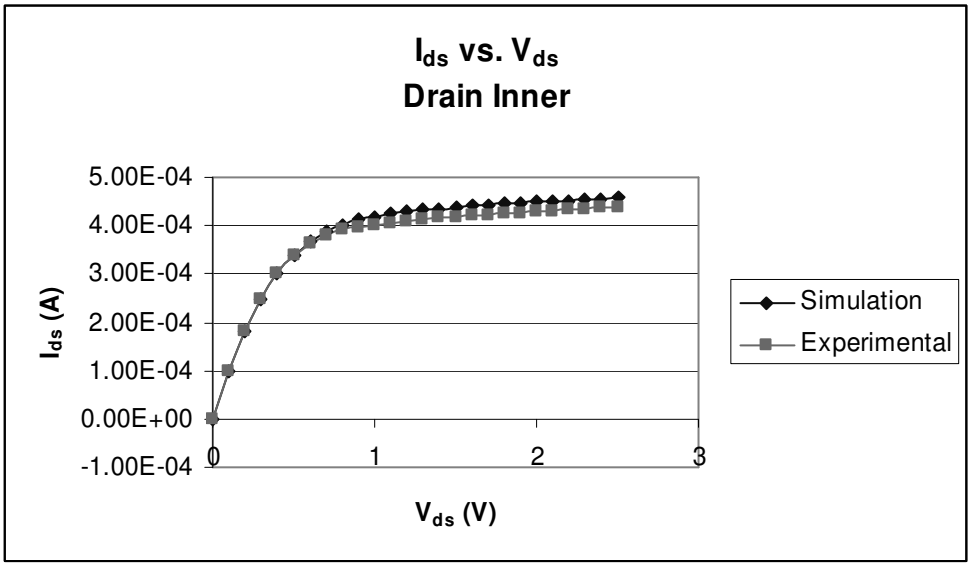

Figure 5.8: I_{ds} vs. V_{ds} for Horseshoe FET with Drain Outer

in R_{out}. No capacitance structures were fabricated for this type of FET, but the capacitance model should provide accurate results for the horseshoe FET as well. No test structures were made of dog bone FETs but the method suggested in section 4.3 can be applied to them as well and should get accuracies similar to that of a horseshoe FET.

5.4 GAS and GAT FET Verification

Because the GAS and GAT FETs show no great advantage over other radiation hardened FETs only one GAS FET's result and one GAT's FET result will be presented. Figures 5.9 and 5.10 show the I_{ds} vs. V_{ds} sweeps for a GAS FET and a GAT FET respectively along with the model results. The two devices were fabricated in the 0.25um process and have a nearly constant gate length of 0.25um. The percent difference for I_{ds}

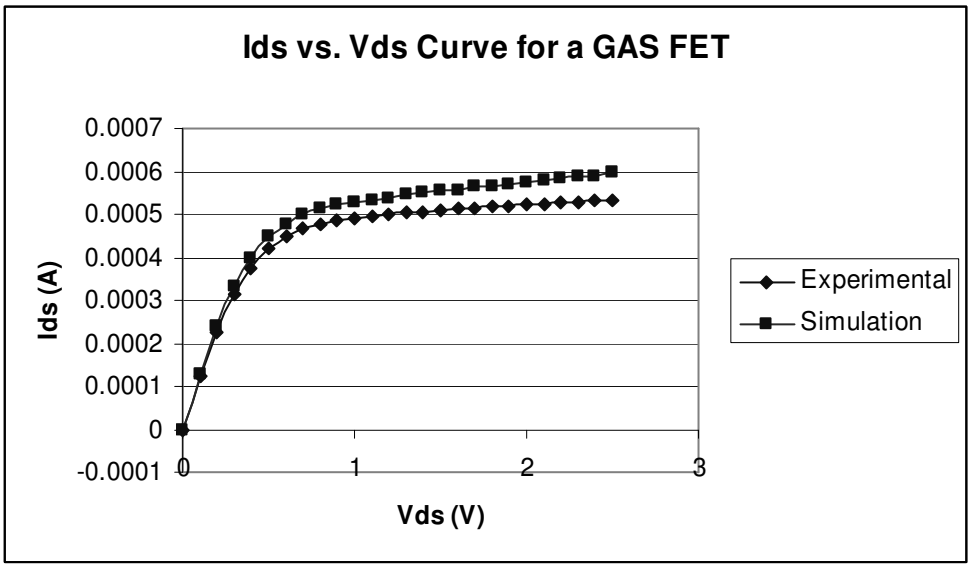

Figure 5.9: I_{ds} vs. V_{ds} for a GAS FET

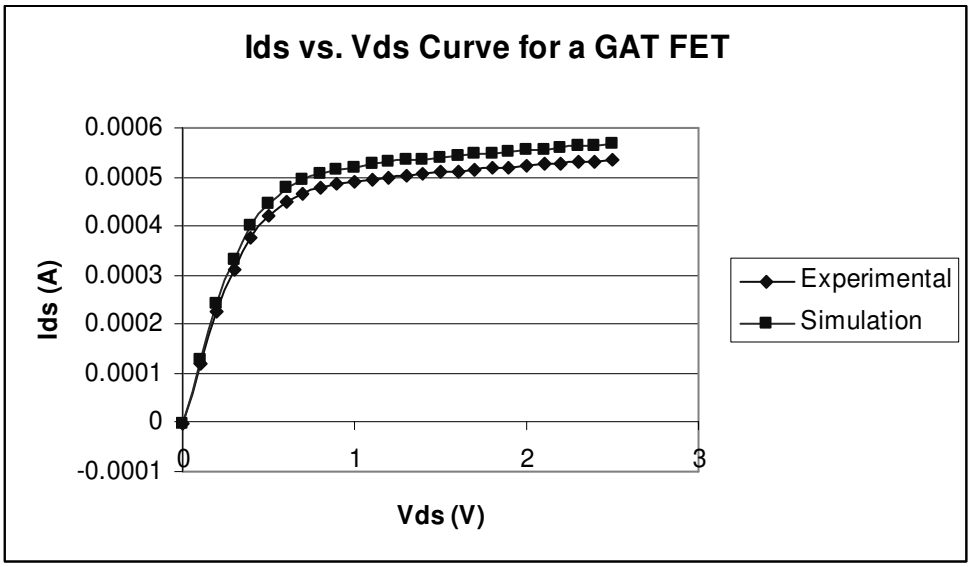

Figure 5.10: I_{ds} vs. V_{ds} for a GAT FET

and in R_{out} is below 20% for all measurements for both types of FETs. A possible reason for the higher errors for these devices, is that some regions of the gate were neglected when dividing the FETs in the multiple sub-circuit shown in Figure 3.4 because it wasn't obvious to which transistor those regions of the gate belonged and how they would behave. Also, the sections similar to half an annular FET were only modeled using the simplified approach and not the more accurate approach.

SECTION SIX

CONCLUSION

In any circuit design, and especially over time as circuits become more complex, it is important to have accurate models so the behavior of fabricated chip will match well to the simulation. Mask and fabrication costs are increasing rapidly as foundries move to smaller and smaller gate geometries and so it is important to get a design right the first time. The behavior of sub-micron devices is more complex and requires more advanced modeling in SPICE. These models have many extracted parameters that define a FET very well, for the nominal process and over the process corners. Designers of circuits required to operate in ionizing radiation environments have suffered the penalty of having poor models when they use abnormal gate geometries to improve radiation tolerance. Errors in the previous models for correcting R_{out}, for an annular FET, often have inaccuracies between 20% and 40% [3]. Typical parameters such as R_{out} should be accurate to within 10% of experimental results to allow accurate simulations. Analog circuits are especially sensitive to the large error in the previous models of FETs with abnormal gate geometries. Some designers use test chips to create a library of well define devices that they will use in their circuit to reduce this error, but they are then limited to those exact gate geometries or must make approximations when deviating from their fabricated geometries. There is also the added cost of designing, fabricating and testing the test chip and the added delay that create problems as well.

This thesis presents a method that can provide accurate results to within 11% in R_{out} and 10% in I_{ds} for the popularly used annular FET. It also provides even more accuracy for a horseshoe shaped FET, which also has increased radiation tolerance.

These small errors were observed on only one wafer for each of the processes, TSMC 0.25um and 0.18um. Also, the errors were further reduced by accounting for the errors measured for a standard FET in the SPICE models. This limited errors to <3% in drain current and output resistance for FETs with a similar gate length. Future work should verify that the majority of the error can be accounted for by process variations as this would suggest. Also, the possible, small, systematic error should be investigated to remove this error.

Additionally, these models were further improved by including how some capacitance parameters should be modified to take into account the abnormal gate geometry used. Some of the changes that were suggested to the SPICE capacitance model parameters were verified with capacitance measurements that were close to the predicted values. The presented modeling the most complete and most accurate models available for any FET with an abnormal gate geometry.

Another advantage is the model creation can be automated, as was done for the results presented, and it can give accurate solutions in a very short amount of simulation time. Describing a given geometry is very simple. Only the corners of the polygon that define the gate need to be provided to the scripts that were created. One popular method for creating more accurate models for FETs with abnormal gate geometries has been to use 3-D simulation tools. The tools can be very complex and take significant setup time for each new gate geometry to be used. Also running an accurate 3-D simulation can take over a day on a fast computer. This is far longer than the typical 5minute. simulation time it takes on a 1GHz computer using the code included in the appendix to get the accurate results shown. This accurate method can not only provide better models

for the described geometries, it allows designers to investigate new geometries that provide advantages to FET parameters and/or radiation tolerance.

This thesis also provided a simple, yet reasonably accurate, way of analyzing different types of FETs that include GAS, GAT and Pi FETs, described in sections 3 and 4. These complex FETs can be split into multiple simple FETs to create a sub-circuit that is easily to created in SPICE. The changes necessary to have the correct device capacitance values for these devices was also presented to make these models complete, except for RF models.

Designers now have the freedom to use other gate geometries for whatever advantage they might provide and have available a method for modeling what the device behavior will be, compared to a standard rectangular FET. Specifically, designers using radiation hardening by design now can have accurate models for the FETs with abnormal gate geometries that they may desire to use for their increased radiation tolerance.

BIBLIOGRAPHY

[1] M. N. Martin and K. Strohbehn, "Analog Rad-Hard by Design Issues", NASA Symposium on VLSI Design, May 2003.

[2] J. L. Andrews, J. E. Schroeder, B. L. Gingerich et al., "Single Event Error Immune CMOS RAM", *IEEE Transactions on Nuclear Science*, vol. 29, no. 6, pp. 2040-2043, December 1982.

[3] G. Anelli, "Conception et Caracterisation De Circuits Integres Resistants aux Radiations pour les Detecteurs De Particules di LHC en Technologies CMOS Submicroniques Profondes," PhD Thesis Submitted to Institut National Polytechnique de Grenoble, 11 December 2000.

[4] J. R. Schwank, "Basic Mechanisms of Radiation Effects in the Natural Space Environment", Notes of the Short Course of the 1994 IEEE Nuclear and Space Radiation Effects Conference, Tucson (Arizona), Section II, pp. 1-109, July 1994.

[5] F. B. McLean, H. E. Boesch, Jr., and T. R. Oldham, "Electron-Hole Generation, Transport, and Trapping in Sio2", in *Ionizing Radiation Effects in MOS Devices & Circuit*s, edited by T. P. Ma and P. V. Dressendorfer, J. Wiley & Sons, New York, 1989.

[6] P. S. Winokur, "Radiation-Induced Interface Traps", in *Ionizing Radiation Effects in MOS Devices & Circuit*s, edited by T. P. Ma and P. V. Dressendorfer, J. Wiley & Sons, New York, 1989.

[7] R. Gaillard, J.-L. Leray, O. Musseau et al., "Techniques de durcissement des composant, circuits, et systemes electroniques", Notes of the Short Course of the 3rd European Conference on Radiation and its Effects on Components and Systems, Arcachon (France), Short Course 3, September 1995.

[8] Grey, Meyer, et al. Analysis and Design of Analog Integrated Circuits-4th ed. New York: J. Wiley and Sons Inc, 2001.

[9] R. C. Lascoe, J. V. Osborn, D.C. Mayer et al., "Total-Dose Tolerance of the Commercial Taiwan Semiconductor Manufacturing Company (TSMC) 0.35-um CMOS Process," *2001 IEEE Radiation Effects Data Workshop*, Vancouver (Canada), pp. 72-76, July 2001.

[10] W. Snoeys, G. Anelli, M. Campbell et al., "Integrated Circuits for particle physics experiments", to be published in the *IEEE Journal of Solid-State Circuit*s, vol. 35, no. 12, December 2000.

[11] A. Giraldo, "Evaluation of Deep Submicron Technologies with Radiation Tolerant Layout for Electronics in LHC Environments", Ph.D. Thesis at the University of Padova, Italy, December 1998.

[12] A. Giraldo, A. Paccagnella, A. Minzoni, "Aspect ratio calculation in n-channel MOSFETs with a gate-enclosed layout", *Solid-State Electronic*s, vol. 44, pp. 981-989, June 2000.

[13] P. Allen and D. Holberg, CMOS Analog Circuit Design. New York: Oxford, 2002.

[14] H. Hatano and K. Doi, "Radiation-tolerant high-performance CMOS VLSI circuit design", *IEEE Transactions on Nuclear Scienc*e, vol. 32, no. 6, pp. 4031-4035, December 1985.

[15] H. Hatano and S. Takatsuka, "Total dose radiation-hardened latch-up free CMOS structures for radiation-tolerant VLSI designs", *IEEE Transactions on Nuclear Scienc*e, vol. 33, no. 6, pp. 4031-4035, December 1986.

[16] P. Grignoux and R. L. Geiger, "Modeling of MOS Transistors with Nonrectangular-Gate Geometries", *IEEE Transactions on Electron Device*s, vol. 29, no. 8, pp. 1261-1269, August 1982.

[17] N. Levinson and R. M. Redheffor, Complex Variables. San Fransisco: Holden-Day, 1970.

[18] D. Johns and K. Martin, Analog Integrated Circuit Design. New York: J. Wiley and Sons, 1997.

[19] "BSIM3 Version 3.2 Manual," Department of Electrical Engineering and Computer Science, University of California, 1998.

[20] Y. Tsividis, Operation and Modeling of the MOS Transistor. New York: McGraw-Hill, 1987.

APPENDIX

A: Matlab Code for Automation

Main script to run the routine for DC modeling:

```
% the global vectors are set by the running of the plot command
% if rplot is replaced with the rplot on the website
global lenvector;  %contains the length of each equal potential line
global larray;   %contains points that define each equal-potential line
global zzzz;     %corners of rectangle geometry is mapped to
global numreim; %number of equal-potential lines to find

numreim=100;
numinmod=10; %newreim must be divisable by this number

%p=polygon([0 .91 .91+2.61i .28+2.61i .25+2.64i .25+3i 3i]);
p=polygon([.27+.79i 1+.79i 1.27+1.06i 1.27+1.79i 1+2.06i .27+2.06i 1.79i
1.06i .24+1.06i .24+1.69i .37+1.82i .9+1.82i 1.03+1.69i 1.03+1.16i .9+1.03i .27+1.03i]);
%p is set to an annular FET

f=rectmap(p);  %creates a rectmap object that defines the mapping between the two
%geometries

%calculates the aspect ratio
ar=(max(imag(zzzz))-min(imag(zzzz)))/(max(real(zzzz))-min(real(zzzz)));

plot(f)  %sets global vectors

%modifies length if averaging is used
lenvector=flipud(lenvector);
newlvec=[];
for k=1:numinmod
   newlvec=[newlvec;mean(lenvector(((k-
1)*numreim/numinmod+1):(k*numreim/numinmod)))];
end
lenvector=newlvec;

%creates vectors for find the distance between equal-potential lines
start=[larray(3)];
stop=[];
temp1=[larray(3)];
temp2=[larray(4)];
for k=5:length(larray)
   if (temp1==0 & temp2==0)
      start=[start;larray(k)];
```

```
      stop=[stop;larray(k-3)];
   end
   temp2=temp1;
   temp1=larray(k);
end
stop=[stop;larray(k)];
distance_start=[sqrt((real(start(1))-real(start(2)))^2+(imag(start(1))-imag(start(2)))^2)];
distance_stop=[sqrt((real(stop(1))-real(stop(2)))^2+(imag(stop(1))-imag(stop(2)))^2)];
for k=2:length(start)-1
   distance_start=[distance_start;(sqrt((real(start(k))-real(start(k-1)))^2+(imag(start(k))-
imag(start(k-1)))^2)+sqrt((real(start(k))-real(start(k+1)))^2+(imag(start(k))-
imag(start(k+1)))^2))/2];
   distance_stop=[distance_stop;(sqrt((real(stop(k))-real(stop(k-1)))^2+(imag(stop(k))-
imag(stop(k-1)))^2)+sqrt((real(stop(k))-real(stop(k+1)))^2+(imag(stop(k))-
imag(stop(k+1)))^2))/2];
end
distance_start=[distance_start;sqrt((real(start(k))-real(start(k+1)))^2+(imag(start(k))-
imag(start(k+1)))^2)];
distance_stop=[distance_stop;sqrt((real(stop(k))-real(stop(k+1)))^2+(imag(stop(k))-
imag(stop(k+1)))^2)];

%sums together distances if averaging is used
newstart=[];
newstop=[];
for k=1:numinmod
   newstart=[newstart;sum(distance_start(((k-
1)*numreim/numinmod+1):(k*numreim/numinmod)))];
   newstop=[newstop;sum(distance_stop(((k-
1)*numreim/numinmod+1):(k*numreim/numinmod)))];
end
distance_start=newstart;
distance_stop=newstop;

dd=flipud(distance_start);
ds=flipud(distance_stop);

%ds=2*ds; %multiply by 2 if only half of geometry is defined
%dd=2*dd;

%Wn=2*lenvector.*ar/numinmod;
Wn=lenvector.*ar/numinmod;
Wi=ds;   %widths found for drain inner
Wo=dd;  %widths found for drain outer

Rdn=1;  %standard fets unit output resistance
```

```
%widthmax=2*ar*lenvector;
widthmax=ar*lenvector; %use full width not just width of region, because may not be a
%narrow channel device

% finds the value for deltaL by calling SPICE and comparing results from when there is
% no effect of CLM and when there is
deltaL=finddeltaL(widthmax,lenvector);

%find the modifier to the output resistance
deltai=(1-(Wi./Wn).*(1-deltaL.*Wn./Wi)./(1-deltaL));
deltao=(1-(Wn./Wo).*(1-deltaL)./(1-deltaL.*Wn./Wo));
Rdi=Rdn.*(1-deltai);
Rdo=Rdn./(1-deltao);

%swap drain inner and outer defined backwards
if mean(Rdi)>mean(Rdo)
   temp=Rdi;
   Rdi=Rdo;
   Rdo=temp;
End

%find widths and lengths iteratively for drain outer device to have correct Rout
[Wo,Lo]=findWL(widthmax,lenvector,Rdo);
Wo=Wo/length(Wo); %normalize

%find PCLM values iteratively to have correct Rout
PCLMi=findPCLM(widthmax,lenvector,Rdi);

%define what PCLM should be for a standard device
PCLMstand=[];
for k=1:length(Wn)
   if lenvector(k) < 0.5  %these regions are defined by over what region the model files
                          %are valid
      PCLMstand=[PCLMstand; %default PCLM value goes here for this size device%];
   elseif lenvector(k) < 1.2
      PCLMstand=[PCLMstand; %default PCLM value goes here for this size device%];
   else
      PCLMstand=[PCLMstand; %default PCLM value goes here for this size device%];
   end
end
%generates results for standard device, drain inner and outer
rs=generateResults2(widthmax,lenvector,PCLMstand,Wn);
ri=generateResults2(widthmax,lenvector,PCLMi,Wn);
ro=generateResults2(widthmax,Lo,PCLMstand,Wo);
```

function [H,RE,IM] = rplot(w,beta,z,c,L,re,im,options)

```
%RPLOT

runningavelen=0;
runningavewid=0;
global lenvector;
global widvector;
global larray;
global warray;
global numreim;
lenvector=[];
widvector=[];
warray=[];
larray=[];
n = length(w);
w = w(:);
beta = beta(:);
z = z(:);
[w,beta,z,corners] = rcorners(w,beta,z);
rect = z(corners);

% Parse input
if nargin < 8
  options = [];
  if nargin < 7
    im = [];
    if nargin < 7
      re = [];
    end
  end
end

Kp = imag(rect(2));
K = rect(1);

% Empty arguments default to 10

if isempty([re(:);im(:)])
  re = numreim;
%re=10;
  im = numreim;
%im=10;
end

% Integer arguments must be converted to specific values
if (length(re)==1) & (re == round(re))
  if re < 1
```

```
    re = [];
  else
    m = re;
    re = linspace(-K,K,m+2);
    re([1,m+2]) = [];
  end
end
if (length(im)==1) & (im == round(im))
  if im < 1
    im = [];
  else
    m = im;
    im = linspace(0,Kp,m+2);
    im([1,m+2]) = [];
  end
end

% Drawing parameters
[nqpts,minlen,maxlen,maxrefn] = scpltopt(options);
qdat = scqdata(beta,nqpts);
%len = max(diff(get(ax(1),'xlim')),diff(get(ax(1),'ylim')));
%minlen = len*minlen;
%maxlen = len*maxlen;
axlim = axis;

%color = 'k';

%vertical lines
for j = 1:length(re)
  % Start evenly spaced
  zp = re(j) + i*linspace(0,Kp,15).';
  new = logical(ones(size(zp)));
  wp = repmat(NaN,length(zp),1);

  % Adaptive refinement to make smooth curve points
  iter = 0;
  while (any(new)) & (iter < maxrefn)
  %  drawnow
    neww = rmap(zp(new),w,beta,z,c,L,qdat);
    wp(new) = neww;
    iter = iter + 1;

   % Add points to zp where necessary
   [zp,wp,new] = scpadapt(zp,wp,minlen,maxlen,axlim);
  end
  wid=0;
```

```
  warray=[warray;0;0;wp];  %add points to width array
  for counterw=1:length(wp)-1
  wid=wid+sqrt((real(wp(counterw))-real(wp(counterw+1)))^2+(imag(wp(counterw))-
imag(wp(counterw+1)))^2);  %calculate running width
  end
  widvector=[widvector;wid];   %add width to vector of width values
  runningavewid=runningavewid+wid;
 % wp
end
avewid=runningavewid/numreim

% horizontal lines...   same but for lengths
for j = 1:length(im)
  % Start evenly spaced
  zp = linspace(-K,K,15).' + i*im(j);
  new = logical(ones(size(zp)));
  wp = repmat(NaN,length(zp),1);

  % Adaptive refinement to make smooth curve
  iter = 0;
  while (any(new)) & (iter < maxrefn)
   % drawnow
    neww = rmap(zp(new),w,beta,z,c,L,qdat);
    wp(new) = neww;
    iter = iter + 1;

    % Add points to zp where necessary
    [zp,wp,new] = scpadapt(zp,wp,minlen,maxlen,axlim);
  end
  larray=[larray;0;0;wp];
  len=0;
  for counterl=1:length(wp)-1
      len=len+sqrt((real(wp(counterl))-real(wp(counterl+1)))^2+(imag(wp(counterl))-
imag(wp(counterl+1)))^2);
  end
  runningavelen=runningavelen+len;
  lenvector=[lenvector;len];
end
avelen=runningavelen/numreim

avewid/avelen
```

function deltaL=finddeltaL(Wn,Ln);

```
deltaL=[];
for k=1:length(Wn)
```

```
   fid=fopen('testL.cir','W');
   addhead(fid);
   if Ln(k) < 0.5
      PCLM=%default PCLM value for this length;
   elseif Ln(k) < 1.2
      PCLM=%;
   else
      PCLM=%;
   end
   addfet(Wn(k),Ln(k),PCLM,1,fid);
   addfoot(fid,'testL.txt');
   fclose(fid);
   %batch call to winspice
   !wspice3 -b testL.cir
   results=readspice('testL.txt');
   deltaL=[deltaL;results(26)/results(15)-1];  %approximate deltaLs from results of sim
end

function addhead(fid);
%add header for making dc measurements

fprintf(fid,'*\n');
fprintf(fid,'vss 6 0 DC 0V\n');
fprintf(fid,'vgsn 5 6 DC 1.5\n');  %can use other voltages
fprintf(fid,'vdsn 4 6 DC 0\n');

function addfet(W,L,PCLM,num,fid);
%add fet with parameters given to file with handle fid

if L < 0.5
%BSIM3 model for FET of length <0.5um
fprintf(fid,'\nmn1 4 5 6 6 CMOSN%d (W=%fu L=%fu)\n\n',num,W,L);
% model values need to be entered
fprintf(fid,'.MODEL CMOSN%d          NMOS   (                 LMIN     = ..\n',num);
fprintf(fid,'+ CALCACM = ..\n');
fprintf(fid,'+LMAX    = ..    WMIN     = ..  WMAX     = \n');
fprintf(fid,'+ LEVEL=  53  TNOM =   XL = \n');
fprintf(fid,'+ AF =  KF = \n');
fprintf(fid,'+XW      =         VERSION  =          TOX      = \n');
fprintf(fid,'+XJ      =         NCH      =       LLN      = \n');
fprintf(fid,'+LWN     =             WLN      =             WWN      = \n');
fprintf(fid,'+LINT    =          WINT     =          MOBMOD   = \n');
fprintf(fid,'+BINUNIT =          DWG      =             DWB      = \n');
fprintf(fid,'+VTH0    =  LVTH0 =  WVTH0    = \n');
fprintf(fid,'+PVTH0   =   K1       =    LK1      = \n');
fprintf(fid,'+WK1     =   PK1      =     K2       =   \n');
```

```
fprintf(fid,'+LK2    =    WK2     =    PK2     = \n');
fprintf(fid,'+K3     =          DVT0    =          DVT1    = \n');
fprintf(fid,'+DVT2   =         DVT0W   =          DVT1W   = \n');
fprintf(fid,'+DVT2W  =          NLX     =          W0      = \n');
fprintf(fid,'+K3B    =          VSAT    =    LVSAT   =    \n');
fprintf(fid,'+WVSAT  =     PVSAT   =    UA      =    \n');
fprintf(fid,'+LUA    =     WUA     =    PUA     =    \n');
fprintf(fid,'+UB     =     LUB     =    WUB     =    \n');
fprintf(fid,'+PUB    =     UC      =    LUC     =    \n');
fprintf(fid,'+WUC    =     PUC     =    RDSW    =    \n');
fprintf(fid,'+PRWB   =          PRWG    =          WR      = \n');
fprintf(fid,'+U0     = LU0     = WU0    = \n');
fprintf(fid,'+PU0    = A0      =    LA0     =    \n');
fprintf(fid,'+WA0    =     PA0     =    KETA    =    \n');
fprintf(fid,'+LKETA  =    WKETA   =    PKETA   =    \n');
fprintf(fid,'+A1     =          A2      =    LA2     =    \n');
fprintf(fid,'+WA2    =     PA2     =    AGS     =    \n');
fprintf(fid,'+LAGS   =     B0      =          B1      = \n');
fprintf(fid,'+VOFF   =   LVOFF   =    WVOFF   =    \n');
fprintf(fid,'+PVOFF  =   NFACTOR =          CIT     =    \n');
fprintf(fid,'+CDSC   =         CDSCB   =          CDSCD   =    \n');
fprintf(fid,'+ETA0   =     LETA0   =    WETA0   =    \n');
fprintf(fid,'+PETA0  =   ETAB    =   LETAB   =    \n');
fprintf(fid,'+WETAB  =   PETAB   =    DSUB    =    \n');
fprintf(fid,'+PCLM   = %f   LPCLM   =    WPCLM   =    \n',PCLM);
fprintf(fid,'+PPCLM  =   PDIBLC1 =      PDIBLC2 =    \n');
fprintf(fid,'+LPDIBLC2=   WPDIBLC2 =     PPDIBLC2 =  \n');
fprintf(fid,'+PDIBLCB =    DROUT   =          PSCBE1   =    \n');
fprintf(fid,'+LPSCBE1 =     WPSCBE1  =     PPSCBE1  =    \n');
fprintf(fid,'+PSCBE2  =        PVAG    =          DELTA    = \n');
fprintf(fid,'+ALPHA0  =     BETA0   =      KT1      =    \n');
fprintf(fid,'+LKT1   =    WKT1    =   PKT1    =    \n');
fprintf(fid,'+KT2    =    LKT2    =    WKT2    =    \n');
fprintf(fid,'+PKT2   =    AT      =         UTE     =    \n');
fprintf(fid,'+LUTE   =    WUTE    =    PUTE    =    \n');
fprintf(fid,'+UA1    =    UB1     =          UC1     =    \n');
fprintf(fid,'+LUC1   =    WUC1    =    PUC1    =    \n');
fprintf(fid,'+KT1L   =      PRT     =          CJ      = \n');
fprintf(fid,'+MJ     =     PB      =    CJSW    = \n');
fprintf(fid,'+MJSW   =   PBSW    = CJSWG   = \n');
fprintf(fid,'+MJSWG  =      PBSWG   =      TCJ     =    \n');
fprintf(fid,'+TCJSW  =   TPB     =    TPBSW   =    \n');
fprintf(fid,'+JS     =        JSW     =        CGDO    =  \n');
fprintf(fid,'+CGSO   =        CAPMOD  =          NQSMOD  =    \n');
fprintf(fid,'+XPART  =         CF      =          TLEV    =  \n');
fprintf(fid,'+TLEVC  =         XTI     =          N       =  \n');
```

```
fprintf(fid,'+HDIF    =        LDIF     =        RSH      =  \n');
fprintf(fid,'+RS      =           RD       =           ACM      =  \n');
fprintf(fid,'+DLC     =       DWC     =       CLC     =  \n');
fprintf(fid,'+CLE     =       ACDE    =          MOIN     =   \n');
fprintf(fid,'+NOFF    =         VOFFCV  =      CKAPPA   =    \n');
fprintf(fid,'+CGDL    =          CGSL     =         CGBO     = \n');
fprintf(fid,'+TOXM    = \n');
fprintf(fid,'+TCJSWG  = ..   TPBSWG   = ..    ALPHA1  = .. )\n');
fprintf(fid,'+OPTACM=..\n');
fprintf(fid,'+THMLEV=..  FLKLEV=..\n\n');

elseif L < 1.2

%FET model for these lengths

else

%FET model otherwise

end
```

function addfoot(fid,fileout);

```
%add footer for making dc measurements

fprintf(fid,'.control\n');
fprintf(fid,'dc vdsn 0 2.6 0.1\n');
fprintf(fid,'print -i(vdsn) > %s\n',fileout);
fprintf(fid,'.endc\n\n');

fprintf(fid,'.end\n');
```

function [Wn,Ln]=findWL(Wn,Ln,Rd);

```
%finds appropriate W and L values by itterating with secant method

for k=1:length(Wn)

   %set up guess 0
   fid=fopen('testWL.cir','W');
   addhead(fid);
   guess0=Ln(k)*Rd(k);
   W0=(Wn(k)/Ln(k))*guess0;
   addfet2(W0,guess0,1,fid);
   addfoot(fid,'testWL.txt');
   fclose(fid);
   !wspice3 -b testWL.cir
   results=readspice('testWL.txt');
```

```
    ans0 = .5/(results(21)-results(16));

    %set up guess 1
    fid=fopen('testWL.cir','W');
    addhead(fid);
    guess1=Ln(k);
    addfet2(Wn(k),guess1,1,fid);
    addfoot(fid,'testWL.txt');
    fclose(fid);
    !wspice3 -b testWL.cir
    results=readspice('testWL.txt');
    ans1 = .5/(results(21)-results(16));  %calc output resistance
    endI = results(9);
    endR = ans1*Rd(k);

    ans0=ans0-endR;
    ans1=ans1-endR;

    %itterate
    newans=endR;
    count=0;

%length secant iteration with nested width secant iteration
    while abs(newans) > .01*endR & count < 100

        newguess = guess1-ans1*(guess1-guess0)/(ans1-ans0);
        Wnew=(Wn(k)/Ln(k))*newguess;
        fid=fopen('testWL.cir','W');
        addhead(fid);
        addfet2(Wnew,newguess,1,fid);
        addfoot(fid,'testWL.txt');
        fclose(fid);
        !wspice3 -b testWL.cir
        results=readspice('testWL.txt');
%getW
        guessW0=Wnew;
        guessW1=0.5*Wnew;
        ansW0=results(9)-endI;
        countW=0;
        fid=fopen('testWL.cir','W');
        addhead(fid);
        addfet2(0.5*Wnew,newguess,1,fid);
        addfoot(fid,'testWL.txt');
        fclose(fid);
        !wspice3 -b testWL.cir
        results=readspice('testWL.txt');
```

```
    ansW1=results(9)-endI;
    newWans=endI;

  while abs(newWans) > .01*endI & countW < 100

    newWguess = guessW1-ansW1*(guessW1-guessW0)/(ansW1-ansW0);
    fid=fopen('testWL.cir','W');
    addhead(fid);
    addfet2(newWguess,newguess,1,fid);
    addfoot(fid,'testWL.txt');
    fclose(fid);
    !wspice3 -b testWL.cir
    results=readspice('testWL.txt');
    newWans = results(9)-endI;
    guessW0=guessW1;
    guessW1=newWguess;
    ansW0=ansW1;
    ansW1=newWans;
    countW=countW+1;
  end
%end getW

    newans = .5/(results(21)-results(16))-endR;
    guess0=guess1;
    guess1=newguess;
    ans0=ans1;
    ans1=newans;
    count=count+1;
  end

  Ln(k)=newguess;
  Wn(k)=newWguess;

end
```

function addfet2(W,L,1,fid); %similar to addfet, but PCLM left at nominal value
%variable num is always set to 1 for this

function P=findPCLM(Wn,Ln,Rd);

```
%finds appropriate PCLM values by itterating with secant method

P=[];
for k=1:length(Wn)

  %set up guess 0
  fid=fopen('testPCLM.cir','W');
```

```
addhead(fid);
guess0=0;
addfet(Wn(k),Ln(k),0,1,fid);
addfoot(fid,'testPCLM.txt');
fclose(fid);
!wspice3 -b testPCLM.cir
results=readspice('testPCLM.txt');
ans0 = .5/(results(21)-results(16));

%set up guess 1
fid=fopen('testPCLM.cir','W');
addhead(fid);
if Ln(k) < 0.5
   PCLM=%guess default value;
elseif Ln(k) < 1.2
   PCLM=   %;
else
   PCLM=  %;
end
guess1=PCLM;
addfet(Wn(k),Ln(k),PCLM,1,fid);
addfoot(fid,'testPCLM.txt');
fclose(fid);
!wspice3 -b testPCLM.cir
results=readspice('testPCLM.txt');
baseRd = .5/(results(21)-results(16));
ans1=baseRd;

endRd=baseRd*Rd(k);
ans0=ans0-endRd;
ans1=ans1-endRd;

%itterate
newans=endRd;
count=0;

while abs(newans) > .01*endRd & count < 100

   newguess = guess1-ans1*(guess1-guess0)/(ans1-ans0);
   if newguess < 0
      newguess = 0.1;
   end
   fid=fopen('testPCLM.cir','W');
   addhead(fid);
   addfet(Wn(k),Ln(k),newguess,1,fid);
   addfoot(fid,'testPCLM.txt');
```

```
        fclose(fid);
        !wspice3 -b testPCLM.cir
        results=readspice('testPCLM.txt');
        newans = .5/(results(21)-results(16))-endRd;
        guess0=guess1;
        guess1=newguess;
        ans0=ans1;
        ans1=newans;
        count=count+1;
    end

    P=[P;newguess];

end

function y=generateResults(Wmax,Ln,PCLM,Wn)
%create final model and gets result
%weighted summing of individual results

y=zeros(26,1);
for k=1:length(Wmax)
fid=fopen('testresult.cir','W');
addhead(fid);
addfet(Wmax(k),Ln(k),PCLM(k),k,fid);
addfoot(fid,'testresult.txt');
fclose(fid);
!wspice3 -b testresult.cir
temp=readspice('testresult.txt')*Wn(k)/Wmax(k);
y=y+temp;
end
```